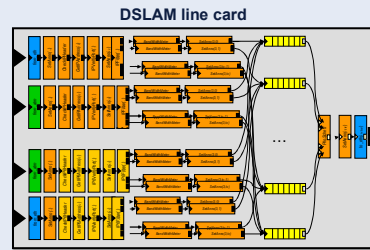


## Motivation & Goal

- Modular platform construction kit to investigate design criteria, such as flexibility, programmability, area, and performance
- Reuse of of-the-shelf components (e.g., programmable embedded cores) and deployment tools where possible
- Refinements (instruction set, co-processors, etc.) where needed as determined by profiling of reference applications
- Synergy: Hardware platform directly supports message passing semantics of application; NoC is a natural choice

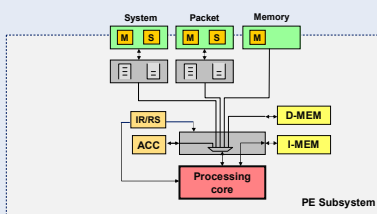
## Application Domain



- Packet processing in access networks
- Data-flow driven processing

- Message passing semantics between computational kernels
- Subject to **tight constraints on costs and performance**
- Flexibility required to support broad variety of protocols and customer requirements

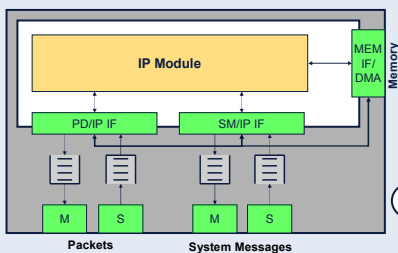
## Network-Optimized Versatile Architecture (NOVA) Platform: Concepts



3

### Systematic development of platform building blocks

- Profiling of embedded general-purpose cores (and their compilers) and specialized packet processing engines
  - Packet processing engines provide high performance; general purpose cores are flexible and have mature compilers
- ⇒ Provides a first estimate of required parallelism



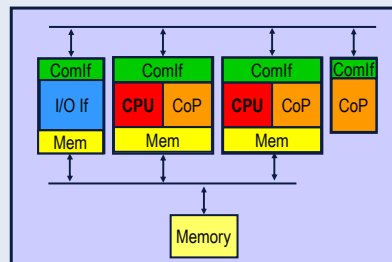
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### NOVA Socket concept

- Homogeneous interface
- Separation of IP-specific interfaces from interconnect and memory interfaces

### 1 Modular platform

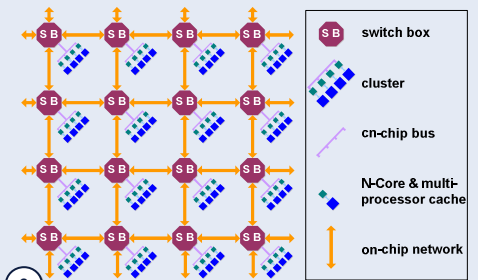
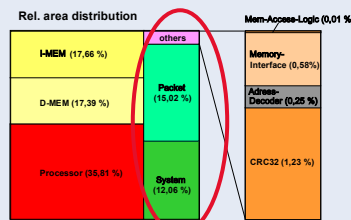
- Number and type of processing cores
- Number and type of co-processors
- Number and type of I/O interfaces
- Heterogeneous memory hierarchy
- Communication architecture



### Efficient implementation

- Two NoC interfaces, buffering 16 64B messages each, need less than 1/3 of the CPU subsystem area

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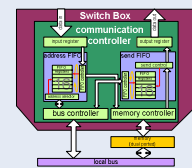
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### GigaNoC – hierarchical Network-on-chip

- Bus-based network for small clusters (< 10 components)
- Switch boxes for connecting clusters

### NoC principles

- Message passing interface with priorities: computation can continue while message is transmitted to destination
- Incorporation of flow control by backpressure signaling to avoid overload and loss
- Lightweight one-word header, which contains destination, message type, and context ID for fast flow-through processing



SoC main components	Area [mm <sup>2</sup> ]		Frequency [MHz]	
	130nm	90nm	130nm	90nm
32 Cores (N-Core)	32 x 0.16	32 x 0.12	205	285
8 switch-boxes (with 5 ports)	8 x 1.125	8 x 0.53	560	650
32 local RAMs (32 KB)	32 x 0.875	32 x 0.875	400	450
8 local packet buffers (2 x 16 KB)	8 x 2 x 0.468	8 x 2 x 0.468		
8 local on-chip buses	8 x 0.05	8 x 0.02	211	290
<b>Total</b>	<b>50.01</b>	<b>43.7</b>	<b>205</b>	<b>285</b>

## Status/Next Steps

- Verification of approach and concepts
- Currently implementing initial NOVA platform prototype comprising approx. 20 message passing clients
- Application-driven analysis using system-level benchmark
- Mapping IP-DSLAM reference application to the platform
- Enables detailed quantitative exploration of design trade-offs
- Demonstrator at CeBIT 2006 trade fair
- Evaluation of GigaNoC for larger systems [2]

## Partners/Funding

### Infineon Technologies

- Communications, Access System Engineering (COM AC SE NP)
- 81726 Munich, Germany
- E-mail: Christian.Sauer@infineon.com

### Heinz Nixdorf Institute

- University of Paderborn, System and Circuit Technology
- Fürstenallee 11, 33102 Paderborn, Germany
- E-mail: niemann@hni.upb.de

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