Frequency Compensation of High-Speed, Low-Voltage CMOS Multistage Amplifiers

Syed Ahmed Aamir*†, Prakash Harikumar*, and J Jacob Wikner*
*Division of Electronics Systems, Department of Electrical Engineering, Linköping University, SE-581 83, Sweden
†Cognitive Interaction Technology - Center of Excellence, Bielefeld University, Bielefeld, Germany
Email: saamir@cit-ec.uni-bielefeld.de, prakash@isy.liu.se, jacob.wikner@liu.se

***Abstract*— This paper presents the frequency compensation of high-speed, low-voltage multistage amplifiers. Two frequency compensation techniques, the Nested Miller Compensation with Nulling Resistors (NMCNR) and Reversed Nested Indirect Compensation (RNIC), are discussed and employed on two multistage amplifier architectures. A four-stage pseudo-differential amplifier with CMFF and CMFB is designed in a 1.2 V, 65-nm CMOS process. With NMCNR, it achieves a phase margin (PM) of 59° with a DC gain of 75 dB and unity-gain frequency (f_{ug}) of 712 MHz. With RNIC, the same four-stage amplifier achieves a phase margin of 84°, DC gain of 76 dB and f_{ug} of 2 GHz. Further, a three-stage single-ended amplifier is designed in a 1.1-V, 40-nm CMOS process. The three-stage OTA with RNIC achieves PM of 81°, DC gain of 80 dB and f_{ug} of 770 MHz. The same OTA achieves PM of 59° with NMCNR, while maintaining a DC gain of 75 dB and f_{ug} of 262 MHz. Pole-splitting, to achieve increased stability, is illustrated for both compensation schemes. Simulations illustrate that the RNIC scheme achieves much higher PM and f_{ug} for lower values of compensation capacitance compared to NMCNR, despite the growing number of low voltage amplifier stages.**

I. Introduction

Due to the continuous scaling of CMOS technologies and the concomitant reduction of supply voltage, output swing as well as intrinsic transistor gain ($g_m r_o$), analog design has become more and more challenging. Among other analog blocks, the operational amplifier, a fundamental building block of most mixed-signal circuits, needs to address this low-gain, low-voltage domain.

In such a low-voltage environment, cascoding to achieve higher gain is no longer feasible. Hence, cascading multiple stages to achieve high gain emerges as a promising design paradigm. Additional amplifier stages, however, introduce poles and zeros that degrade stability and makes advanced frequency compensation indispensable. Several compensation schemes such as Nested Miller Compensation [1] (NMC), Nested Gm-C Compensation [2] (NGCC), Active Feedback Frequency Compensation [3] (AFFC) and many others have been proposed. A majority of the publications on multi-stage amplifier compensation schemes targets low-speed, high-capacitive load applications where the GBW is less than 10 MHz. However, detailed comparison of compensation schemes with respect to the amplifier specifications such as phase margin, f_{ug} and DC gain is often not available for high-speed amplifiers in deep submicron CMOS processes.

In this paper, we compare NMCNR [4] and RNIC [5] compensation techniques using the schematic level implementation results for two different multistage amplifiers. The first amplifier is a four-stage pseudo-differential architecture described in Section II, while the second one is a three-stage single-ended amplifier discussed in Section IV. The application of the compensation schemes and corresponding results are explored in Section III and Section IV.

II. Four-stage OTA architecture

The four-stage amplifier is a pseudo-differential design, which eliminates the tail current source in the input differential pair and becomes particularly suited for low-voltage design [6]. The four-stage fully symmetric amplifier with a cross-coupled input stage designed in a 1.2-V, 65-nm CMOS process [7] is shown in Fig. 1. The amplifier is fully differential (without a tail current source) with common-mode feedforward (CMFF) and common-mode feedback (CMFB), both applied simultaneously for stable output common-mode. The four gain stages of the amplifier are distributed in the form of two separate two-stage OTAs, each of which also detects the input common-mode of the OTA at a node V_{cm} using separate stages. Hence each OTA will act as output common-mode detector of its preceding OTA, and can feed this detected common-mode "back", to apply the CMFB technique. In Fig. 1, the V_{cmNext} node (in the second OTA) is fed back to fix the output common-mode of the first OTA using devices M_{3a} and M_{4a}. CMFF is applied by controlling the output bias transistor M_3 using the detected common-mode V_{cm}.

The input stage has a positive feedback cross-coupled NMOS load, which is used to attain higher gain than the g_{m1}/g_{m2} previously available from the positive feedback-less input stage. This will also increase the node capacitance contributing towards two nearby poles (f_{p2}, f_{p3}) caused by the total parasitic node capacitance. The other two poles include the non-dominant pole - due to the parasitic capacitance at the ouput of the first OTA - and the dominant pole from the output load C_L (f_{p4}, f_{p1}). The presence of the four-pole system within this amplifier scheme is further stabilized using two compensation schemes as explained in the following section.

III. Stabilization of the four-stage OTA

The design of the four-stage OTA was primarily targeted for high bandwidth, high gain applications. The design process

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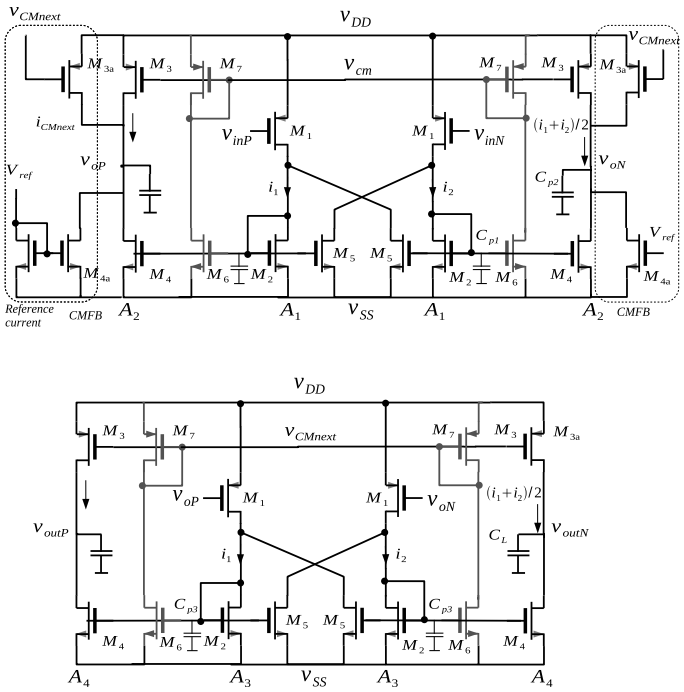

Fig. 1. Schematic of the four-stage OTA.

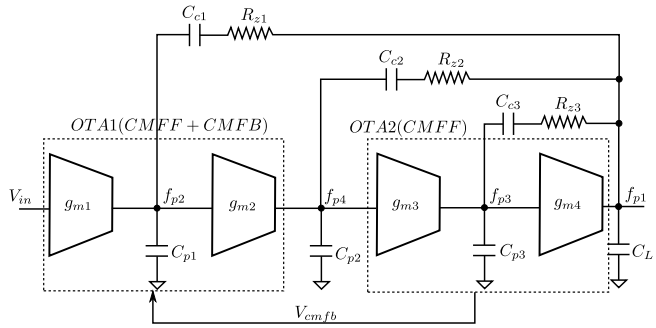

Fig. 2. Block diagram of four-stage OTA with NMCNR

TABLE I
POLE LOCATIONS OF FOUR-STAGE OTA WITH NMCNR.

Compensation	f_{p1}	f_{p2}	f_{p3}	f_{p4}	f_{ug}
None	6.01e7	5.05e8	5.16e8	1.31e9	3.3e9
NMC (1C)	1.49e6	1.13e9	5.16e8	1.31e9	2.1e9
NMCNR (1C1R)	1.47e6	1.8e9	5.16e8	1.31e9	2.6e9
NMC(2C)	2.41e6	1.24e8	5.16e8	1.5e9	1.1e9
NMCNR (2C2R)	2.41e6	1.55e8	5.16e8	7.82e8	2.4e9
NMC(3C)	1.28e5	8.96e7	3.51e8	2.4e9	582.3e6
NMCNR (3C3R)	1.28e5	9e8	3.54e8	2.33e9	804e6

and analysis indicated the presence of four poles clustered together, causing higher degree of unstability (PM is essentially negative). To stabilize this four pole system, we performed a careful analysis of the equivalent small-signal models, and further applied NMCNR and RNIC schemes.

A. NMCNR stabilization

NMCNR [4] applied to the four-stage OTA is shown in Fig. 2. Starting with the uncompensated amplifier with four poles, the innermost capacitive loop in Fig. 2 would split the dominant pole f_{p1} from pole f_{p2} to bring f_{p1} lower in frequency and f_{p2} further higher than f_{p3}. Closing the next loop (R_{z2}, C_{c2}) splits mostly the pole f_{p4} from the pole f_{p2}, pushing the latter much lower in frequency. The final Miller loop (R_{z1}, C_{c1}) involves the input stage of the OTA and the associated parasitic pole (f_{p3}) which was unmoved so far, is pushed lower in frequency along with f_{p1} and f_{p2} while f_{p4} is pushed to more than three times the unity-gain frequency (f_{ug}). The dominant pole, the three non-dominant poles and the f_{ug} before and after NMCNR compensation are given in Table I. It illustrates the effect of adding each Miller feedback loop on the pole locations. Here NMC(1C) describes the case when only the innermost Miller capacitor has been added, while NMCNR (1C1R) indicates a nulling resistor added in series with that capacitor and so on. The reduction in f_{ug} which accompanies each level of nesting in the NMC scheme is evident. The pole locations for the four-stage OTA shown in Fig. 2 is given by the NMCNR (3C3R) case. Thus NMCNR achieves pole-splitting and creates a dominant-pole at a much lower frequency than in the uncompensated case. The NMCNR four-stage OTA achieves DC gain = 75 dB, f_{ug} = 712 MHz, and PM = 59°. The gain-phase plot is shown in Fig. 3.

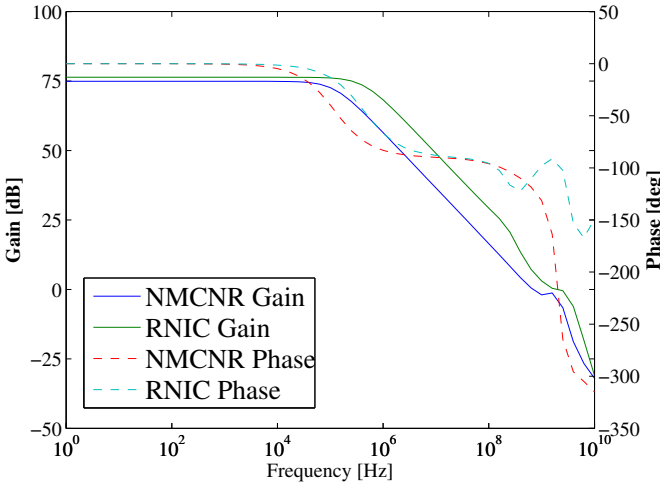

Fig. 3. Gain-phase plots of the four-stage OTA.

B. RNIC stabilization

Saxena et al. proposed a compensation technique which utilized split-length transistors to create a low impedance node for connecting the Miller capacitor [8]. The compensation scheme does not require an embedded cascode in the input pair to create a low impedance node. A split channel length achieves the same topology, in which one "half" of the transistor is always in triode region. Therefore, it is also suitable for low-voltage implementation. Indirect feedback through the low impedance node eliminates the RHP zero and improves PM. The block diagram of the four-stage OTA with RNIC is

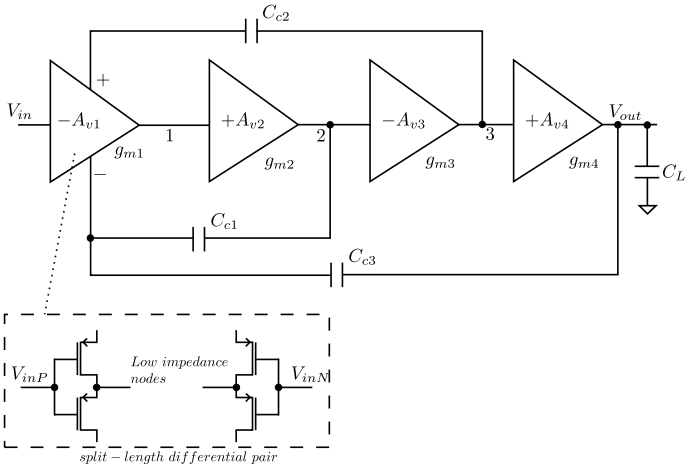

Fig. 4. Block diagram of the four-stage OTA with RNIC.

TABLE II
POLE LOCATIONS OF FOUR-STAGE OTA WITH RNIC.

Compensation	f_{p1}	f_{p2}	f_{p3}	f_{p4}	PM(°)
None	9.8e-5	1.87e-4	6.67e7	6.5e8	-111
RNIC(1C)	1.87e-4	1.16e7	6.67e7	6.5e8	4
RNIC(2C)	1.87e-4	2.19e6	6.16e7	6.67e7	75
RNIC(3C)	4.31e5	1.31e8	1.61e8	1.37e9	85

shown in Fig. 4. The schematic of the four-stage OTA with RNIC technique for stability is shown in Fig. 5. As shown, the input-differential pair uses split-length transistors, where the top PMOS will be in triode and the bottom PMOS in saturation with V_{Zp} and V_{Zn} being the low-impedance nodes. The compensation capacitances are connected to the low-impedance nodes in a manner that ensures negative feedback between the OTA stages. In order to determine the pole-

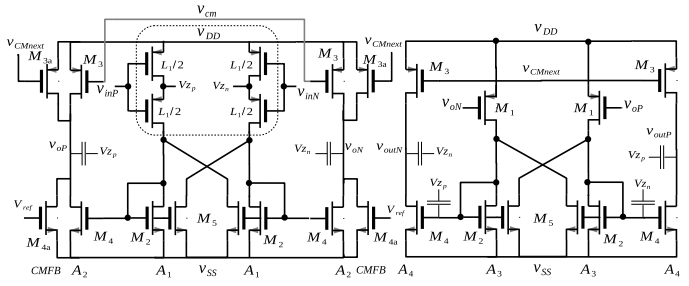

Fig. 5. Schematic of the four-stage OTA with RNIC.

splitting achieved by RNIC, a small-signal model of the four-stage OTA equivalent to the transistor schematic shown in Fig. 5 was utilized. Simulations on the small-signal equivalent model illustrates the effect of RNIC as given in Table II.

The RNIC compensated four-stage OTA (based on schematic level results) achieves DC gain = 76 dB, f_{ug} = 2 GHz and PM = 84°. The gain-phase plot is shown in Fig. 3.

IV. THREE-STAGE OTA

The 40-nm CMOS node has transistors with intrinsic gain lower than those of 65-nm process and uses a supply voltage of

TABLE III
POLE-ZERO LOCATIONS OF THREE-STAGE OTA WITH RNIC.

RNIC	f_{p1}	f_{p2}	f_{p3}	f_{p4}	f_{p5}	f_{z1}	f_{z2}
None	2.3e7	3.1e8	3.3e8	8e10	-	4.1e10	-
2C2R	5.4e4	2.4e8	1.3e9	8.5e9	4e11	1e8	1e9

1.1 V. Since 40-nm processes are increasingly being adopted for SoC implementations, high-gain amplifiers also become necessary in the analog and mixed-signal blocks. In this work, a three-stage OTA has been designed in a 1.1-V, 40-nm CMOS process. The OTA architecture utilizes differential pairs for the first and second stages followed by a common-source amplifier acting as the third stage [5]. Use of a differential pair as the second-stage simplifies biasing.

A. RNIC stabilization

The schematic of the three-stage OTA with RNIC is shown in Fig. 6. Split-length differential pair in the first-stage creates the low-impedance nodes (fbl, fbr). A reversed nested compensation topology is employed to avoid the output node being loaded by the two compensation capacitors and help achieve higher f_{ug}. There are two compensation loops, each with a capacitor and series resistor. The transfer function of the three-stage OTA has two LHP zeros (f_{z1}, f_{z2}) and five poles $f_{p1} - f_{p5}$ [5]. Of these, f_{p4}, f_{p5} are caused by the low-impedance nodes and lie at very high frequencies, while f_{p2}, f_{p3} can be canceled using the LHP zeros by properly choosing R_{1c} and R_{2c} [5]. Thus addition of the series resistors helps to accomplish pole-zero cancellation and improves the PM. The amplifier can also be stabilized without using the series resistors for pole-zero cancellation. But fixing the location of poles and zeros proves more tedious and the resulting PM might be lower. The three-stage OTA achieves DC gain = 80 dB, f_{ug} = 770 MHz and PM = 81°. The gain-phase plot of the three-stage OTA with RNIC is shown in Fig. 7.

A small-signal equivalent model was set up to analyse the impact of RNIC on pole-zero locations and the results are provided in Table III. It highlights the pole-splitting and shows how the non-dominant poles f_{p2} and f_{p3} are located close to the zeros f_{z1} and f_{z2} respectively. Also the pole-zero pairs, f_{p2}, f_{z1} and f_{p3}, f_{z2} are closely located. Such an arrangement of non-dominant poles and LHP zeros is optimal for a low-power three-stage amplifier [5].

B. NMCNR stabilization

The three-stage OTA was compensated using NMCNR. Since the feedforward current through the compensation capacitor creates a RHP zero, the PM is degraded. Higher values of compensation capacitance compared to the RNIC case will also be required. The location of poles and zeros before and after NMCNR is shown in Table IV. f_{z2} is a RHP zero which degrades the phase margin. The gain-phase plot is shown in Fig. 7.

TABLE IV

POLE-ZERO LOCATIONS OF THREE-STAGE OTA WITH NMCNR.

NMCNR	f_{p1}	f_{p2}	f_{p3}	f_{p4}	f_{z1}	f_{z2}
None	2.4e7	3.4e8	8.3e8	-	-	-
2C2R	3.4e4	3.6e7	1.2e9	4.5e9	4e7	4.1e8*

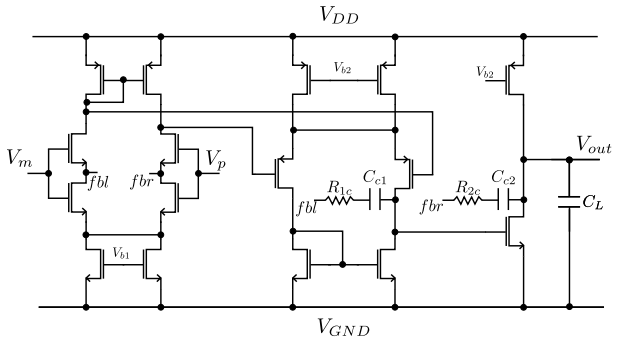

Fig. 6. Schematic of the three-stage OTA with RNIC.

V. COMPARISON OF NMCNR AND RNIC

A comparison of both the schemes is summarized in Table V while Table VI compares this work with recently published high-speed multistage amplifiers. Both table entries refer to the four-stage and three-stage OTAs by I, II respectively whereas NR and RI denote NMCNR and RNIC. The total load capacitances for the two OTAs (OTA-I and OTA-II) were 2 pF and 1 pF respectively. C_t and R_t are the total compensation capacitance and resistance used in each topology. It is evident from Table V that the RNIC schemes achieves higher f_{ug} as well as PM, while requiring the same (or lower) values of compensation capacitance. Further, Table V also suggests that the RNIC requires lower power compared to NMCNR, for the same target design specifications. From Table VI, it is evident that our designs had to rely on multiple gain stages to target higher gain in modern low voltage process nodes. Despite this we maintain much higher phase margin and offer considerable bandwidth using RNIC techniques.

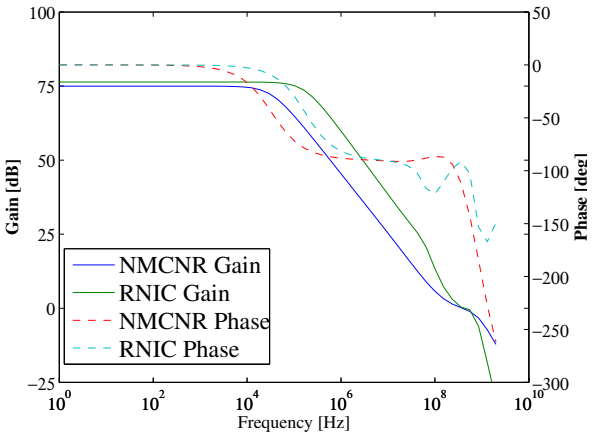

Fig. 7. Gain-phase plots of the three-stage OTA.

TABLE V

COMPARISON OF NMCNR AND RNIC.

OTA	C_t (pF)	R_t kΩ	f_{ug} (MHz)	PM	Gain	Power
I-NR	3.05	1.5	712	59°	75 dB	11.2 mW
I-RI	3.4	-	2000	84°	76 dB	13.6 mW
II-NR	8	1.4	396	64°	75 dB	3 mW
II-RI	4.5	0.77	770	81°	80 dB	2.6 mW

TABLE VI

COMPARISON WITH RECENT HIGH-SPEED MULTISTAGE AMPLIFIERS.

Spec.	[9]	[10]	[11]	I-RI	II-RI
Process (nm)	120	130	130	65	40
Supply (V)	1.2	1.2	1.2	1.2	1.1
Stages	2	2	3	4	3
C_L (pF)	3.2	4	0.6	2	1
PM (°)	45	60.5	62	84	81
f_{ug} (MHz)	1500	319	11000	2000	770
Gain (dB)	40.4	84	39.5	76	81

VI. CONCLUSION

Four-stage and three-stage amplifiers have been designed in 65-nm, 40-nm CMOS process for high-speed applications. The amplifiers have been stabilized using NMCNR and RNIC schemes. Transistor-level simulations indicate that RNIC achieves higher phase margin, f_{ug} values than NMCNR for comparable values of compensation capacitance. Thus the RNIC scheme achieves higher power efficiency and reduced chip area compared to NMCNR.

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