Neuromorphic Circuits for Short-Term Plasticity with Recovery Control

Harshawardhan Ramachandran[1], Stefan Weber[1], Syed Ahmed Aamir and Elisabetta Chicca
Faculty of Technology, Cognitive Interaction Technology - Center of Excellence, Bielefeld University
33619 Bielefeld, Germany
Email: rharshawardhan@techfak.uni-bielefeld.de

***Abstract*—We present real-time neuromorphic VLSI circuits that implement the synaptic dynamics of Short Term Plasticity (STP). STP supports useful signal processing computational primitives such as change detection and gain control. Compact circuits implementing these mechanisms play a key role in providing neuromorphic VLSI systems with autonomous adaptation capabilities. We propose two different, flexible, short-term adaptation CMOS circuits for controlling the efficacy of synapses in response to incoming spikes. These circuits can be configured to either implement short-term depression or facilitation, with independent control over the adaptation and recovery rates. Our results demonstrate the dynamic properties of the proposed circuits and their behaviour in the frequency domain.**

I. INTRODUCTION

Nervous cells exhibit a multitude of adaptation mechanisms at all functional levels, from soma to dendrites, to synapses, on a myriad of time scales [1]. On short time scales, an important adaptive response is observed at the level of the synapses and often referred as Short Term Plasticity (STP). The resulting synaptic modification is temporary, and depends mainly on the pre-synaptic activity. The synaptic strength decreases (increases) in response to each incoming action potential giving rise to Short Term Depression (STD) (Short Term Facilitation (STF)). The depletion of neurotransmitters at a pre-synaptic cell causes depression, whereas calcium influx after spike generation increases the release probability, giving rise to facilitation [2], [3]. During inter-spike intervals, a recovery mechanism drives the synaptic efficacy to its resting value on a timescale of hundreds of milliseconds to seconds.

On the computational level, STD has been implicated in dynamic gain control mechanisms in cortical synapses, since it suppresses the synaptic response in a frequency-dependent manner [4]. It can be used to implement spike frequency adaptation as well as directional selectivity [5]. Furthermore, STP can be used to implement filters in the frequency domain: low frequency components can be filtered out by STD [6], while STF can act as a high pass filter. A post synaptic neuron receiving both STD as well as STF-based inputs can therefore demonstrate bandpass properties [7]. Despite a plethora of literature on STP modeling, there are few real-time neuromorphic implementations with flexible synaptic dynamics. In the accelerated-time domain, a leaky Integrate-and-Fire (IF) model with a large dynamic range of slow/fast facilitation and depression in conductance based synapses is presented in [8]. Similarly, [9] utilizes an STP circuit to compensate for the inhomogeneities of neuromorphic VLSI devices with self-adjusting networks.

For real-time implementations, an STD circuit for a simple static synapse using only three transistors, and one capacitor was presented in [10] and further analyzed in [11]. This circuit is often used to control the weight of a Differential-Pair Integrator (DPI) synapse circuit [12]. Its main limitation is the lack of independent, linear control over the recovery time-constant (effective during inter-spike intervals). A circuit with flexible and independent control over the depression strength and recovery time constants would allow the implementation of different forms of STD, such as the sudden depression followed by fast recovery observed in auditory pattern recognition in cricket phonotaxis [13]. Implementing such temporal dynamics using the real-time neuromorphic circuits proposed in [10] is challenging due to lack of control over the recovery time-constant.

In this paper, we solve the above mentioned problem by presenting two real-time neuromorphic circuits for modeling STD or STF which provide independent control over the recovery rate and can be tuned to better match theoretical models. In the following sections we describe both STP circuits, categorized on the basis of their recovery behavior, and present their response in the frequency domain.

II. SIMPLE STP CIRCUIT

Fig. 1 shows a simple and compact circuit for STP with independent control over depression strength and recovery time constants. The output voltage of the circuit, V_{out}, is supposed to control the weight bias of a synaptic circuit (e.g. the DPI [12]) by means of three transistors and one capacitor. Four parameters are used to independently set the rate of adaptation and recovery, the resting level of the synaptic weight and its steady-state depressed (facilitated) boundary level. Fig. 1a shows the STD circuit: V_{wei} and V_{tau} control the gate voltages of the transistors M_2 and M_3 respectively, and are set such that the circuit is operated in the sub-threshold regime. Upon the arrival of a pre-synaptic pulse, the capacitor C_w is charged through the path created by transistor M_1 and M_2, at a rate controlled by the bias voltages V_{wei} and V_{tau} for the duration of the input pulse. During inter-spike intervals, transistor M_3 tries to discharge C_w back to its resting charge at a rate controlled by the bias voltage V_{tau}.

During an input pulse, the net current flowing into the capacitor is given by the difference between the current flowing through M_3 and the current flowing through $M_{1,2}$. At the

[1]Authors equally contributed to this work.

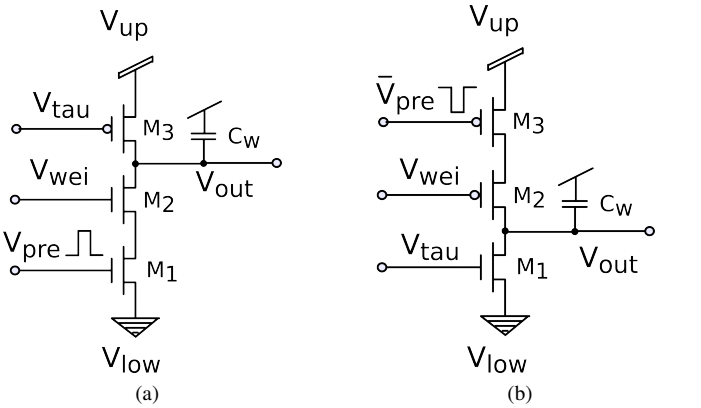

Fig. 1: Simple STP circuits: (a) STD circuit. Upon the arrival of a pre-synaptic spike on V_{pre}, the capacitor C_w is charged by an amount of charge which depends linearly on the pulse duration and the charge current (which is an exponential function of V_{wei}). V_{tau} control the recovery toward the resting level which is set by V_{up} in absence of input spikes. V_{low} sets the steady state boundary level.

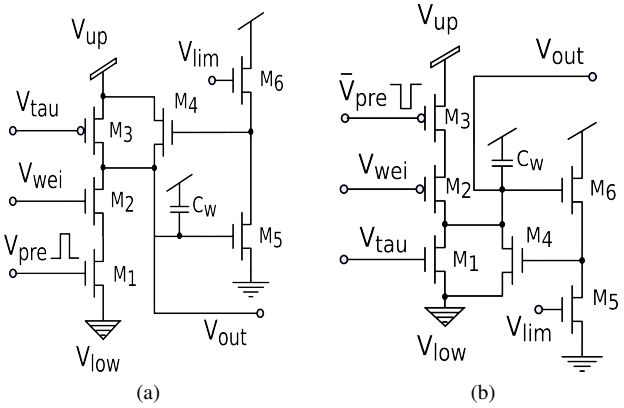

Fig. 2: Feedback STP circuits: (a) STD circuit. (b) STF circuit. V_{up}, V_{low}, V_{pre}, V_{wei} and V_{tau} work in the same way as in the simple STP circuits. V_{lim} adjusts the negative-feedback current through M_4.

stimulus onset situation (the output is at its resting voltage and the first input pulse is provided), we can assume that transistor M_2 is saturated (provided the difference between V_{up} and V_{low} is large enough). At the arrival of the first input spike, we can assume that $I_{M_3} << I_{M_2}$ then the output voltage becomes:

$$C_w \frac{V_{out}(t)}{dt} = -I_{n0} e^{\frac{\kappa_n V_{wei} - V_{low}}{U_T}}$$

After the pulse, only the positive current will be active and the output voltage will be driven towards its resting state:

$$C_w \frac{V_{out}(t)}{dt} = I_{p0} e^{\frac{-\kappa_p V_{tau} + V_{up}}{U_T}} \left(1 - e^{\frac{V_{out}(t) - V_{up}}{U_T}}\right)$$

The steady state condition is reached when the charge accumulated during a spike is equal to the charge removed during the inter-spike interval. This happens due to two reasons: 1. The V_{ds} voltage of M_2 decreases, reducing the charge current. 2. V_{ds} of M_3 increases, increasing the discharge current.

The STF circuit shown in Fig. 1b is the complementary version of the STD circuit. During an input pulse the net current flowing into the capacitor is given by the difference between the current at M_1 and the current flowing through $M_{2,3}$. If we consider a stimulus onset, we can assume that transistor M_2 is saturated (provided a large enough difference between V_{up} and V_{low}). V_{up} in Fig. 1b is much higher than V_{up} in Fig. 1a, which is required to make the circuit stay in sub-threshold region. This circuit needs to be operated within the input range of the DPI synaptic circuit [12] (which is much less than V_{up}), a constraint that keeps M_2 always saturated. This situation prevents the circuit to reach the steady state, when dynamics demand a sharp increase and decrease in V_{out}. If M_1 gets saturated after an input spike and if the charge per inter-spike interval provided through M_2 is smaller than the charge per spike removed through M_3, then V_{out} would not reach the steady state. However, the circuit could be useful for applications of less stringent temporal dynamics, e.g. for limited boundary conditions.

Compared to the widely used STD circuit described in [10], this circuit substitutes the highly non-linear 'adaptive element' [14] (a p-type diode with its bulk connected to its source) for controlling the temporal dynamics of the short-term plasticity mechanism with a simple transistor with tunable gain. The advantages are a much more compact layout (since the 'adaptive element' requires a separate well), the possibility of implementing the complementary circuit for STF, and the complete control of the temporal dynamics. To overcome the limitations observed in this STF circuit, we modified our circuit by adding a negative feedback as described in the next section.

III. Feedback STP circuit

The transistors in the circuit proposed in the previous section leave their saturated regimes to reach the steady state depressed/facilitated point. As shown later in Sec. IV, for a given input frequency, the circuit reaches the steady state depressed/facilitated level only for a specific set of parameters, limiting the possible range of STP dynamics. To avoid this dependency, we introduced a negative feedback loop in our design. The feedback allows to adjust the steady state weight independently from the input frequency and the number of spikes required to reach the steady state potential. Further, it allows to vary the transient response of the circuit without modifying its capacitance. The circuits for STD and STF are shown in Fig. 2. The feedback is implemented using a source follower circuit whose output is connected to the gate of a second recovery transistor (M_4 in Fig. 2a and Fig. 2b) connected in parallel to the original one.

Since the problems for the circuit presented in Sec. II are more pronounced for the facilitation case, we will describe the effect of the feedback in the STF circuit. The STD circuit works in a comparable way. The added devices M_5 and M_6 both operate in sub-threshold saturation region and form a source follower circuit with the linear transfer function $V_g = \kappa_n(V_{out} - V_{lim})$, where V_g is the gate voltage of M_4. The current drawn from the capacitor C_w through M_4 rises exponentially with the charge of the capacitor, thus forming a negative feedback loop. This replaces the non-saturation operation of M_5 and M_2, so that the voltage V_{out} reaches a

steady state even with fully saturated sub-threshold transistors. If the transistors M_1, M_2 and M_4 are operated in saturation, the equation describing V_{out} following one spike of duration t_{pw} and an arbitrary recovery time t is:

$$CV_{out}(t) = CV(0) + I_{M_2}t_{pw} - I_{M_1}t - \int_0^t I_{M_4}(V_{out}(t'))dt'$$

Steady state is reached when $V_{out}(\frac{1}{f_{in}}) = V(0)$. The integral is not analytically solvable without further assumptions. However, it provides an intuitive understanding for the qualitative dynamics of the circuit. Assuming a constant positive inter spike charge difference $I_{M_2}t_{pw} - \frac{I_{M_1}}{f_{in}}$, the output voltage rises linearly per spike until:

$$\int_0^{\frac{1}{f_{in}}} I_{M_4}(V_{out}(t'))dt' = \int_0^{\frac{1}{f_{in}}} I_{n0}e^{\frac{\kappa_n(V_{out}(t')-V_{lim})-V_y}{U_T}}dt'$$

is strong enough to settle the difference. The saturation condition is not necessarily fulfilled, but it should be the regular use case, as the feedback is provided by M_4.

If the input charge per spike $I_{M_2}t_{pw}$ is significantly greater than the constant $\frac{I_{M_1}}{f_{in}}$ the steady state is most notably determined by V_{lim}. So we can use V_{lim} to provide the limitation for the highest steady state voltage (in this configuration V_{up} sets the recovery for small frequencies). This also provides a smoother feedback than the sudden cut-off given by the non-saturation transistors in both Sec. II and [10], resulting in a wider bandwidth of intermediate states between the lowest steady state voltage and the highest one. The layout for this circuit, however, is bigger than the other circuits as 3 transistors have to be added.

IV. RESULTS AND DISCUSSION

We designed the proposed circuits using a standard 350 nm CMOS process, and analyzed their transient behavior with Spectre® simulator. The synaptic parameters were swept for a given constant input spike frequency (100 Hz) and pulse width (1 μs). Fig. 3 shows the simulation results for the circuit described in Sec. II, for several values of the bias parameters V_{tau} and V_{wei}. The voltages V_{up}, V_{low}, the capacitance and the input frequency are set to operate the circuit within the input range of the DPI synapse.

The parametric curves of Fig. 3 show that both the STD and STF circuits reach the steady state level only for a subset of parameters, limiting the dynamic range of the circuit and the flexibility in setting the synaptic weight. This problem is more pronounced in the STF circuit because both the M_2 and M_3 transistor are in saturation region, and the steady state is not reached within the simulation time. All STD curves (except for one) reach the steady state by retaining one of the transistors (with gate voltages V_{tau} or V_{wei}) in saturation. The response of the feedback STP circuit by sweeping V_{wei} and V_{tau} is not shown in the paper as it is similar to the simple STP circuit. The influence of V_{lim}, however, is shown in Fig. 4 where the linear output behaviour of the added source follower results in a linear variation of the steady state voltage, without influencing the initial rise.

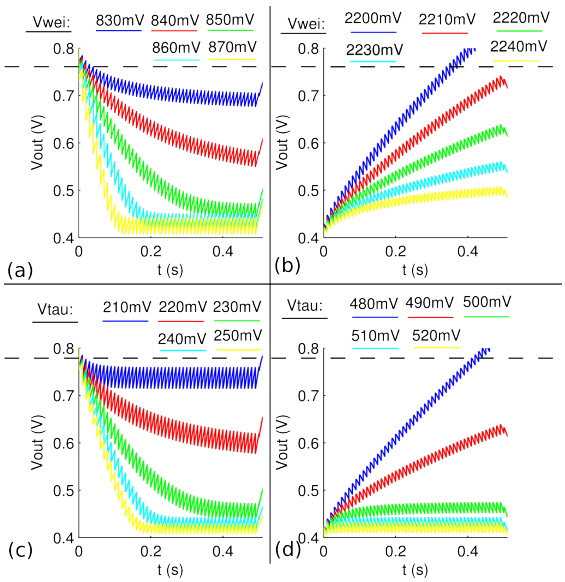

Fig. 3: Parametric sweep of STD (left) and STF (right) in response to a train of spike with constant input spike frequency (100 Hz) and pulse width (1 μs): (a) and (b) show the change in V_{out} with respect to the change in V_{wei}. (c) and (d) show the change in V_{out} with respect to the change in V_{tau} for both simple STD and STF circuits of Sec. II respectively. In both STD plots the steady state is not reached within the simulation time for one value of the parameter. In the STF plots, the steady state is not reached for a number of different parameters.

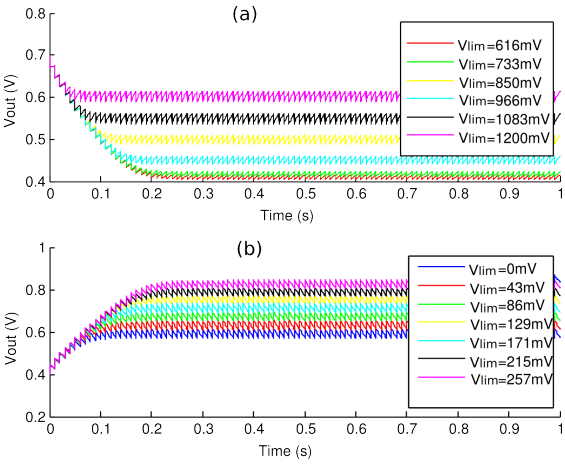

Fig. 4: Effect of the feedback on STP for the STD (a) and STF (b) circuits of Sec. III. The linear change of behaviour in the steady state voltage is clearly visible in the range from 850 mV to 1200 mV for STD and in the whole range for STF. A steady state V_{out} approaches the limit (V_{low} or V_{up}).

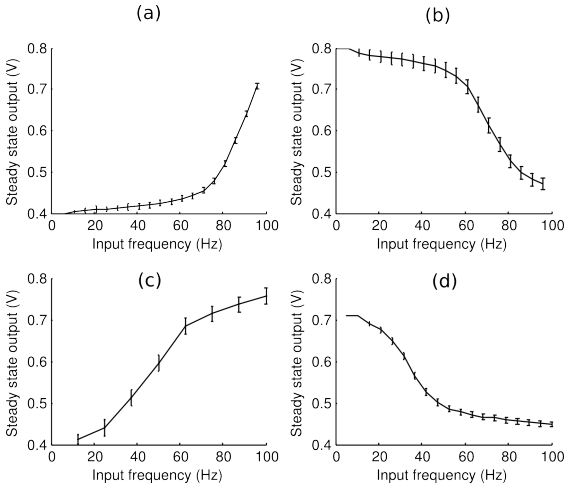

Fig. 5: Steady state output voltages for increasing input frequencies in (a) STF and (b) STD circuits of Sec. II as well as (c) STF and (d) STD circuits of Sec. III. For the simple STF circuit, the output voltage at the end of stimulus onset (0.5 s) is selected as steady state output voltage, even though it did not converge for the entire input frequency band and some steady state voltages cannot be reached with any given frequency input. STD exhibits a low-pass response while STF shows a high-pass response.

The steady state output voltage for swept spike frequencies for all presented circuits are plotted in Fig. 5 showing the high-pass and low-pass filtering properties of STF and STD respectively, by spanning over the entire operation range (between V_{up} and V_{low}). Each point in the curve represents the average of mean voltages during the inter spike intervals when steady state is reached. The error-bars represent the mean standard deviation from the mean inter spike voltage. The top left plot (Fig. 5) of simple STF circuit has not converged within the simulated time interval, so the last mean inter spike voltages are chosen as steady state values. On the other hand, a clear convergence is exhibited by feedback STF circuit in the bottom left curve. The inverse proportionality obtained between the steady state amplitudes and the input spike frequencies are comparable to the results presented in [10].

The bandwidth can be adjusted by varying the difference between the currents controlled by V_{wei} and V_{tau}, while the upper limit where higher frequencies lead to higher weight can be limited by V_{lim}. A decreasing V_{tau} controlled current or an increasing V_{wei} controlled current moves the weight change to lower frequencies. Since the maximum output voltage for a constant input and decay current only depends on V_{lim}, it is possible to find sets of parameters to obtain the desired temporal dynamics with low restrictions on the value of C_w.

V. Conclusion

We presented two compact circuits for the implementation of short term plasticity that provide independent control over the weight change as well as the recovery. This increases the applicability in cases where the absolute weight range should be independent from the temporal dynamics. A simple and very compact circuit allows the straightforward implementation of STP. The range of parameter sets converging against the steady state, however, is highly limited. This renders the STF version of the circuit unsuitable for many cases. Adding a negative feedback to the circuit solves the problem, leading to the design of flexible STD and STF (with complementary versions of the same circuit). The proposed feedback STF circuit can easily be connected with its STD counterpart to share most of the transistors and their capacitance and thus save layout space. A digital select input can activate the desired behaviour. This gives us the flexibility of choosing and tuning the temporal dynamics of STP in a desired way.

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