Development of a low noise analog readout for a DEPFET pixel detector

DISSERTATION
zur Erlangung des Grades eines Doktors
der Naturwissenschaften

vorgelegt von

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eingereicht beim Fachbereich Physik
der Universität Siegen

Siegen 2003

Gutachter der Dissertation: Prof. Dr. M. Holder
Prof. Dr. P. Buchholz

Datum der Disputation: 23. Januar 2004

Internetpublikation der Universität Siegen: urn:nbn:de:hbz:467-459

To my wife Dana and my children
Cristiana and Andrei

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by
Adrian Sorin Niculae

Abstract: Silicon pixel detectors have become very popular in a large variety of applications such as experimental particle physics, medical imaging, video and digital cameras. The DEPFET pixel detector is a novel concept of a silicon detector consisting of a JFET transistor integrated on a fully depleted silicon substrate. The signal charge generated by an ionizing particle within the detector substrate is collected at the transistor gate by means of a special depletion scheme called sideward depletion. From the gate, the signal charge modulates directly the JFET channel current. The current signal is further amplified and processed by external electronics. The internal amplification mechanism ensures low noise, even at room temperature. The electrical charge is removed from the JFET gate by a clear mechanism. Two possible clear methods have been suggested: pulsed clear and continuous clear.

In the present work, DEPFET structures with continuous clear mechanism have been studied. A low noise analog readout circuit has been developed in CMOS technology. This readout chip has been tested with different DEPFET pixel structures. By recording energy spectra of known radioactive sources, an electronic noise of about 13 e^- has been measured at room temperature. The DEPFET device opens therefore new possibilities for applications that require very good energy resolution at room temperature.

Contents

Chapter 1

Introduction

The progress in experimental high energy physics (HEP) has pushed the development of more refined techniques in detector physics. Semiconductor detectors have been used for more than twenty years for the detection of ionizing particles. In the meantime the semiconductor detectors have found their application also in consumer electronics (digital cameras, video camcorders based on CCD[1] sensors), in medicine (tomographic systems) or in astrophysics (x-ray and γ-ray cameras)

The most widely spread material for semiconductor detectors is silicon. The reasons for it are that its material structure is very well understood, it generates a natural oxide (SiO_2) with nearly the same lattice parameters (important for the fabrication of structures such as MOS[2] transistors) and last but not least, the fabrication costs are relatively low.

The simplest semiconductor detector consists of a $300\mu m$ thick silicon substrate with a diode structure formed on one side. By applying a large reverse voltage, the silicon substrate is depleted of free charge carriers and becomes sensitive to ionizing particles (e.g. high energy charged particles, photons). The signal charges generated by such particles in the detector substrate can be detected as current pulses at the diode node.

To obtain information about the position of the particle hit, the diode structure is fabricated in form of narrow strips (strip detectors) or small rectangular cells (pixel detectors). The input capacity of these detectors is however large and limits the energy resolution of the detector. An improvement in the energy resolution is obtained by employing the principle of sideward depletion [Gat84]. Using this technique, large area detectors can be depleted without having a large capacitance at the input node. The noise performance and therefore the energy resolution is substantially improved, as it is the case of the silicon drift detector (SDD) [Str00, Lec01] or the *pn*-CCD structure [Str95].

The energy resolution can be further increased by integrating a preamplifier directly on the detector. The detectors in this category are called DEPFET[3] devices [Kem87, Ces96, Kle96] and consist basically of a field effect transistor integrated on a fully depleted substrate. The signal charge is collected underneath the transistor channel and from there, like a transistor internal gate, it controls the channel current. To avoid the overfilling of the internal gate with thermally generated charges, these are cleared out permanently

[1] Charge Coupled Device
[2] Metal Oxide Semiconductor
[3] DEPleted Field Effect Transistor

(continuous clear devices) or at regular time intervals (pulse clear devices). A noise of ENC[4]$\approx 5e^-$ at room temperature has been reached with a pulse-clear DEPFET detector [Ulr01].

In the present work, the performances of the DEPFET device with continuous clear mechanism are presented. In contrast with the pulse clear DEPFET which, like a CCD structure, is an integrating detector (it collects the charge during a fixed time interval), the continuous clear DEPFET is a detector which is always sensitive and responds individually to each incoming particle. An analog readout for the DEPFET detector has been developed as a dedicated ASIC[5] chip in $0.6\mu m$-CMOS (Complementary MOS) technology. The noise performance of the detector-readout system is tested by recording energy spectra from radiative sources of known energy. The DEPFET device can find various applications in High Energy Physics or in the x-ray astronomy, but also in the medicine or in the field of x-ray spectroscopy.

The work is divided in eight chapters. After this short introduction, the interaction of radiation with matter (with emphasis on silicon detectors) is briefly reviewed in this chapter.

The second chapter presents the working principle of the DEPFET detector. The investigated DEPFET structures are also described here. The static measurements of the various DEPFET structures are shown in chapter 3.

Chapter 4 deals with the small-signal and the noise analysis of the DEPFET detector with continuous clear mechanism. The theoretical noise calculations of the DEPFET device are presented here.

The fifth chapter describes the building blocks of the readout circuit. Results of the circuit simulation are also shown in this chapter. The fabricated chip is measured at first without the detector and the results are presented in chapter 6. Chapter 7 shows the noise measurements of the detector-readout system. The noise performances are evaluated from the measured energy spectra of different radioactive sources.

The summary and the conclusion of the results of this work are presented in the last chapter. An outlook towards further improvements and possible application fields is also given here.

1.1 Interaction of radiation with matter

Radiation sees matter in terms of its basic constituents, i.e. an aggregate of electrons and nuclei. The way in which the radiation interacts with these constituents depends on the type of radiation, its energy and the type of material. For charged particles and photons, electromagnetic interaction is the most common process. For neutrons however, strong interaction processes are preferred. In the following discussion, only the interaction of charged particles and photons with matter will be considered.

[4]Equivalent Noise Charge
[5]Application Specific Integrated Circuit

1.1.1 Interaction of charged particles with matter

When a charged particle passes through matter it interacts with its constituents via the Coulomb force. There are two main processes that characterize the interaction mechanism. On one side, the particle is deflected from its incident direction due to the elastic scattering on nuclei. On the other hand, the particle loses energy mainly due to inelastic collisions with the atomic electrons of the material. For relativistic particles, other processes like the emission of Cherenkov and transition radiation or bremsstrahlung also contributes to the energy loss.

The mean energy loss dE per length dx of a charged particle due to ionization is described by the Bethe-Bloch formula [Gru96]:

$$-\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 \rho z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[ln\left(\frac{2m_e c^2\beta^2\gamma^2}{I}\right) - \beta^2 - \frac{\delta}{2}\right] \tag{1.1}$$

where

N_A	-	Avogadro number (6.022×10^{23} atoms/mol)
r_e	-	classical electron radius (2.817×10^{-13} cm)
m_e	-	electron mass
c	-	speed of light
z	-	charge of incident particle in units of elementary charge
Z,A	-	atomic number and atomic weight of the absorbing material
ρ	-	mass density of the absorbing material
I	-	mean excitation potential (characteristic of the absorber)
β	-	v/c of the incident particle
γ	-	$(1-\beta^2)^{-1/2}$
δ	-	density correction: $\delta \approx 2ln\gamma + \zeta$, where ζ is a material constant

The mean energy loss of an α-particle and a proton in silicon are plotted in Figure 1.1 as a function of the kinetic energy $E_k = Mc^2(\gamma - 1)$. The correction factor δ was neglected here.

At low (non-relativistic) energies, the mean energy loss is dominated by the factor $1/\beta^2$ and decreases with increasing velocity. At $\beta \approx 0.96$ a minimum energy loss is reached. Particles which correspond to this minimum are called *minimum ionizing particles* (MIP). The minimum energy loss is the same for all the particles with the same charge. The energy deposited by a MIP in a 300 μm thick silicon detector is approximately 120 keV.

At high (relativistic) energy the mean energy loss increases with the energy, as the logarithmic term in equation 1.1 becomes large.

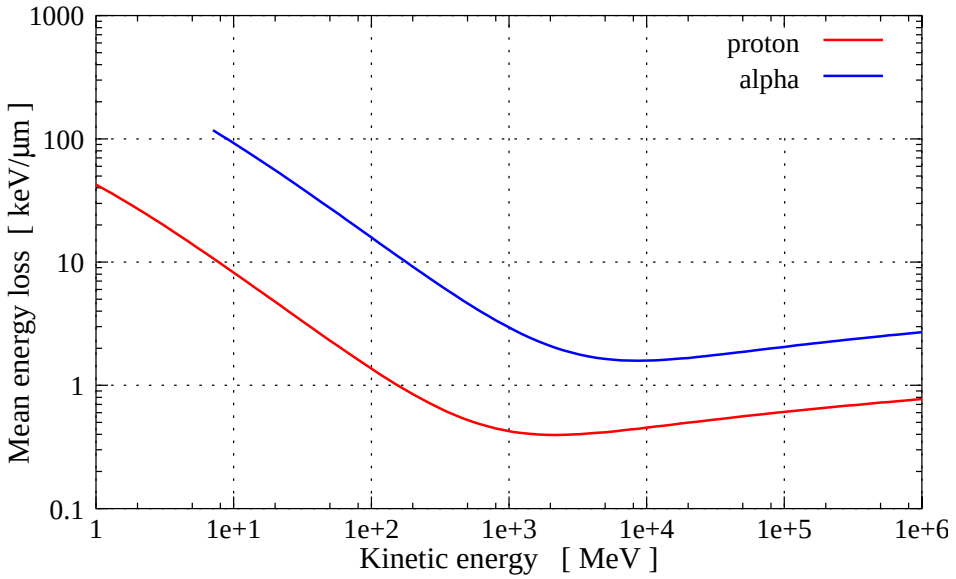


Figure 1.1: Rate of energy loss of a proton and an α-particle in silicon.

1.1.2 Interaction of photons with matter

The interaction of photons (x-ray and γ-rays) with matter is fundamentally different from that of charged particles. In particular, the photon's lack of an electrical charge makes impossible the inelastic collisions with the atomic electrons. Instead, the main interactions of x-rays and γ-rays in matter are: photoelectric effect, Compton scattering and pair production. Depending on the photon energy, one or other of these interaction processes is dominant.

Photoelectric effect

The photoelectric effect involves the absorption of a photon by an atomic electron and the subsequent ejection of the electron from the atom. The energy of the outgoing electron is:

$$E_e = E_\gamma - E_b = h\nu - E_b \tag{1.2}$$

where $E_\gamma = h\nu$ is the incident photon energy and E_b is the electron binding energy. Since free electrons cannot absorb photons for reasons of momentum conservation, the photoelectric effect occurs always on bound electrons, while the recoil momentum is absorbed by the atomic nucleus. The probability of photoelectric absorption on a K-shell electron is particularly large due to the proximity of the nucleus, regarded as the third collision partner.

The ejected electron interacts with the electrons from neighboring atoms and deposits its energy by means of ionization. A hole created in an atomic shell will be occupied by an electron from an outer shell. An amount of energy equal to the difference between the two levels will be released in form of a fluorescence photon or an Auger electron. These are again absorbed by the detector material and almost the entire energy of the

incident photon is deposited in the detector. In case that the secondary (fluorescence) photon escapes the detector, an additional line (the so-called *photo-escape* line) occurs in the photon energy spectrum at an energy of approximately $h\nu$ - E_K (E_K is the binding energy of the electron in the K-shell). For silicon, $E_K = 1.84keV$.

For photon energies $E_\gamma \gg E_K$, the cross section for the photoelectric effect is approximately proportional to Z^n (Z-atomic number) where $n = [4 \div 5]$, and inverse proportional to $E_\gamma^{7/2}$ [Leo94]. The higher Z materials are therefore the most favored for the photoelectric absorption of high energy γ-rays.

Compton scattering

Compton scattering is one of the best understood processes in photon interactions. The Compton effect describes the elastic scattering of photons on free electrons. The electrons in matter are of course bound. If the photon energy is high with respect to the electron binding energy, the latter can be neglected and the electrons can be considered free.

The scattering process is illustrated in Figure 1.2. The incident photon γ with the

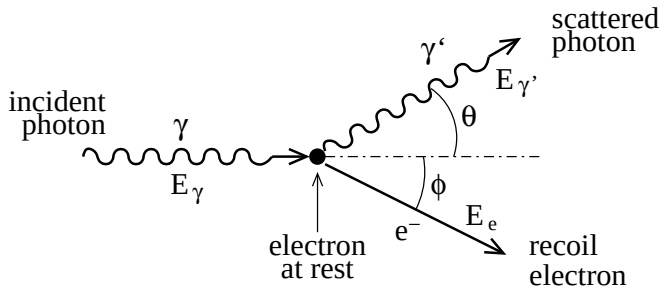


Figure 1.2: Compton effect on free electron.

energy E_γ hits an electron at rest and is deviated from its initial direction at an angle θ. Following the energy and momentum conservation, the electron recoils in a specific direction (angle ϕ) with the energy E_e. Applying energy and momentum conservation, the following relations are obtained:

$$\begin{aligned} E'_\gamma &= \frac{1}{1+\varepsilon(1-cos\theta)} E_\gamma \\ E_e &= E_\gamma - E'_\gamma \\ cot\phi &= (1+\varepsilon) tan\frac{\theta}{2} \end{aligned} \tag{1.3}$$

where E'_γ is the energy of the scattered photon and $\varepsilon = E_\gamma / m_e c^2$. The maximum scattering angle of the electron is $\phi_{max} = 90^o$ while the maximum angle for the scattered photon is $\theta_{max} = 180^o$. A maximum energy transfer occurs at this angle and the corresponding electron energy is given by:

$$E_e^{max} = \frac{2\varepsilon}{1+2\varepsilon} E_\gamma \tag{1.4}$$

E_e^{max} is called the Compton edge.

The probability for Compton scattering is typically small, but at energies around 1 MeV, the Compton effect is the dominant process in photon interaction. The energy distribution of the Compton electrons is derived from the Klein-Nishina formula [Kle29]. The differential cross-section of the Compton effect with respect to the electron energy is given by:

$$\frac{d\sigma}{dE_e} = \frac{\pi r_e^2}{m_e c^2 \varepsilon^2}\left[2 + \frac{s^2}{\varepsilon^2(1-s^2)} + \frac{s}{1-s}\left(s - \frac{2}{\varepsilon}\right)\right] \tag{1.5}$$

where $s = E_e/E_\gamma$. Figure 1.3 shows the energy distribution of the Compton electrons for three different energies of the incident photon.

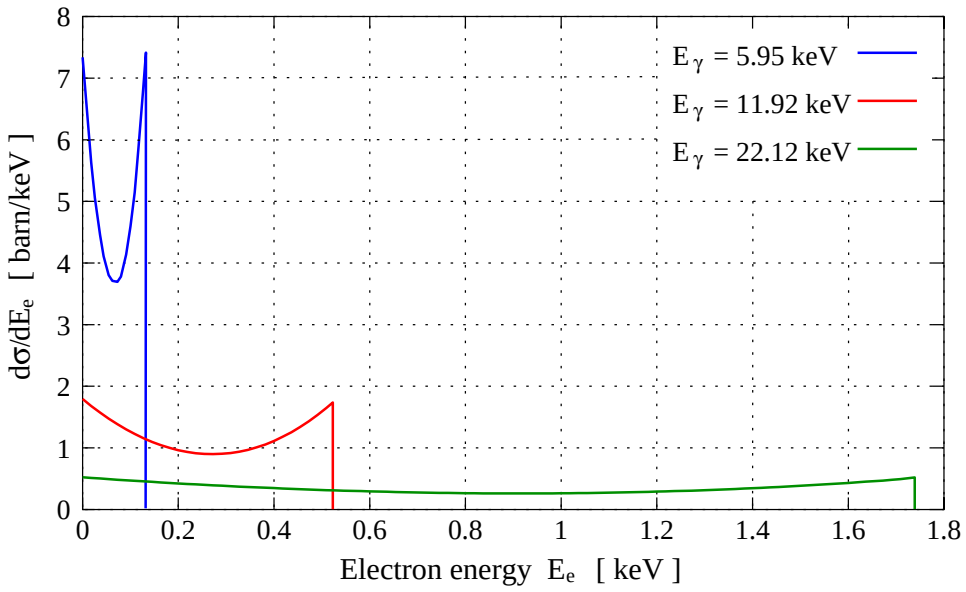


Figure 1.3: Energy distribution of the Compton electrons for three different energy values of the incident photon.

In silicon detectors, the Compton effect becomes dominant over the photoelectric effect at photon energies larger that $\approx 80keV$ (see Figure 1.4).

Pair production

In the process of pair production, the incident photon is absorbed in the Coulomb field of the nucleus and an electron-positron pair is released. For this reason, the pair production occurs only for photon energies at least twice the rest energy of the electron (511 keV). As a consequence, the pair production process plays a role only for high energetic photons (starting from the MeV range).

Figure 1.4 shows the probability of photon interaction in silicon as a function of the photon energy. For energies up to $\approx 100keV$ the dominant process is the photoelectric

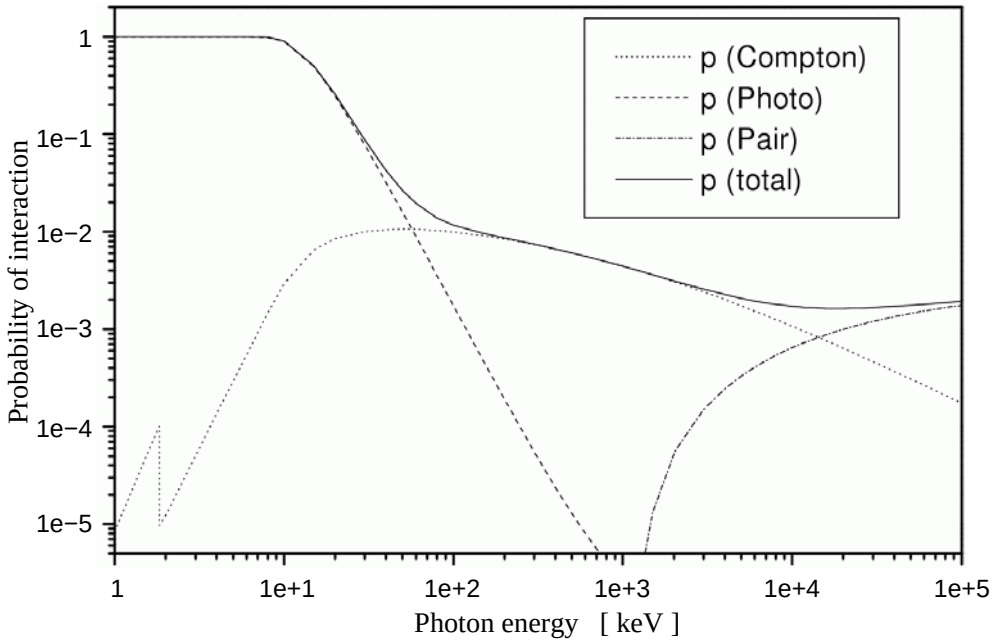


Figure 1.4: Interaction probability of photons in silicon as a function of energy [Nees00].

effect. The Compton effect plays the dominant role for energies between 100 keV and 10 MeV, where the pair production becomes the significant interaction process.

Chapter 2

The DEPFET principle

The building principle of the DEPFET detector [Kem87], [Ces96] is described in this chapter. The structure consists basically of two elements: the detector substrate and a JFET transistor integrated directly on the detector (**DEPFET**- DEPleted Field Effect Transistor). In the following sections each of these elements is described separately. The way in which both elements are integrated in a single structure is also shown here. Furthermore, the structures which are used to clear out the signal charges from the detector are presented in this chapter. The layout of the investigated DEPFET structures is shown at the end of the chapter.

2.1 The *p*-*n* junction diode

The detection part of the DEPFET detector consists of a p-n junction diode. The properties of such an interface between a p-type and an n-type semiconductor material are used in the most semiconductor detectors. Figure 2.1a shows an idealized p-n junction at equilibrium, i.e. no external voltage is applied on the device.

The junction consists of a p-type (doped with acceptor atoms) semiconductor material brought together with an n-type (doped with donor) semiconductor. The practical realization of a junction is more complex than shown here, special techniques must be used to form such a device [Leo94].

When the two types of semiconductors are brought together, the holes which are major charge carriers in the p-type material diffuse into the n-type region where they are in minority. The same happens with the electrons (major charge carriers in the n-type material) which diffuse into the p-type region. The diffusion process leaves back negative ions in the p-type semiconductor and positive ions in the n-type region. As a consequence, an electrical field gradient is created across the junction (the field is maximum at the interface). This field stops the diffusion process, the system reaches an equilibrium state and a region of immobile space charge is left about the interface (between $-x_p$ an x_n in Figure 2.1b). This region is called *depletion zone* or *space-charge region*.

Using Maxwell's equations, the electrical field distribution as well as the electrical potential distribution can be easily calculated [Sze81]. These quantities are plotted in Figure 2.1c and Figure 2.1d. It can be seen that a potential difference occurs across the junction. This potential difference is called *built-in* or *contact* voltage. Denoting the

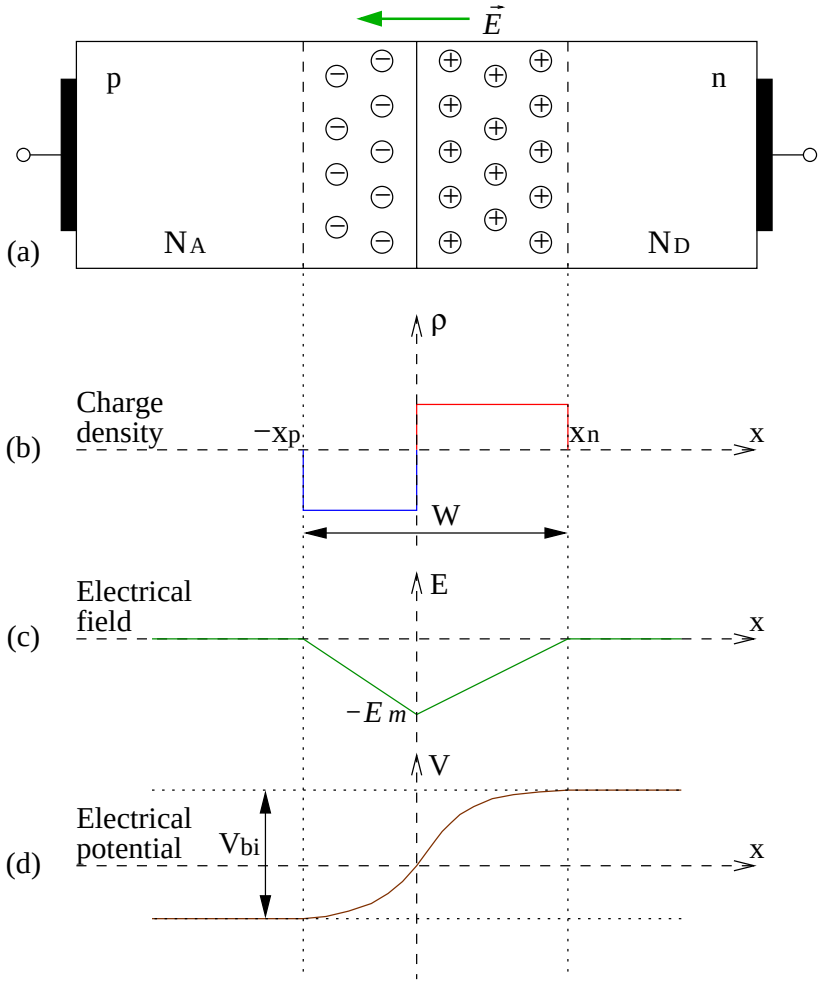


Figure 2.1: (a) p-n junction at equilibrium; (b) Charge density distribution across the junction; (c)Electrical field distribution across the junction; (d) Electrical potential distribution across the junction.

acceptor and donor impurity concentrations as N_A and N_D respectively, the expression of the built-in voltage is given by:

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.1}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the electron charge and n_i is the intrinsic carrier concentration in the semiconductor material.

The width of the depletion zone W is given by:

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_{bi}} \tag{2.2}$$

where ϵ_s is the electrical permittivity of the semiconductor material. The extensions of

the depletion zone in the p-region and in the n-region are:

$$x_p = \left(\frac{N_D}{N_A + N_D}\right) W \qquad\qquad x_n = \left(\frac{N_A}{N_A + N_D}\right) W \tag{2.3}$$

In practice, the impurity concentration in one part of the junction is chosen much higher (several orders of magnitude) than in the other part. The resulting junction is called *one-sided abrupt* junction. Let us assume the case of a p^+-n junction, i.e. $N_A \gg N_D$. The depletion zone extends only into the n-region (from equations 2.3: $x_p \approx 0$, $x_n \approx W$) and equation 2.2 becomes:

$$W = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}V_{bi}} \tag{2.4}$$

2.1.1 The reverse biased p^+-n junction as a particle detector

Now consider the case of a p^+-n junction biased with a constant reverse voltage, i.e. the potential at the p^+-contact is negative with respect to the potential at the n-contact. The applied voltage has the same sign as the built-in voltage and adds to it. As a consequence, the width of the depletion depletion zone increases as equation 2.4 becomes now:

$$W = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(V_{bi} + V_r)} \tag{2.5}$$

where V_r is the magnitude of the applied reverse voltage. If the applied voltage is much larger than the built-in voltage, the later can be neglected and the width of the depletion region becomes proportional to the square-root of the applied voltage.

From equation 2.5 one can obtain the reverse voltage which is needed to deplete entirely a p^+-n junction detector of thickness d:

$$V_r = d^2\frac{qN_D}{2\epsilon_s} \tag{2.6}$$

As a numerical example, assume a Si detector of 300 μm thickness with the homogeneous doping concentration of the n-substrate of $N_D = 2 \cdot 10^{12} cm^{-3}$. The reverse voltage which has to be applied in order to fully deplete the detector substrate is then $V_r \approx 140V$.

The properties of the depletion zone are particularly attractive for radiation detection. Let us consider the Figure 2.2 where a p^+-n junction is biased with a reverse voltage $-V_r$. The electrical field and potential distribution across the junction are also plotted in the figure. If V_r is large enough (given by the equation 2.6), the whole detector substrate is depleted and becomes sensitive to ionizing particles. When such a particle crosses the detector, electron-hole pairs are generated within the depleted substrate by means of ionization processes. Due to the electrical field distribution across the structure, the holes drift to the negative contact (the p^+-side), while the electrons will drift to the positive contact (n^+-side). Thus, an electrical current proportional to the deposited energy in the detector flows across the device and can be detected with appropriate electronics.

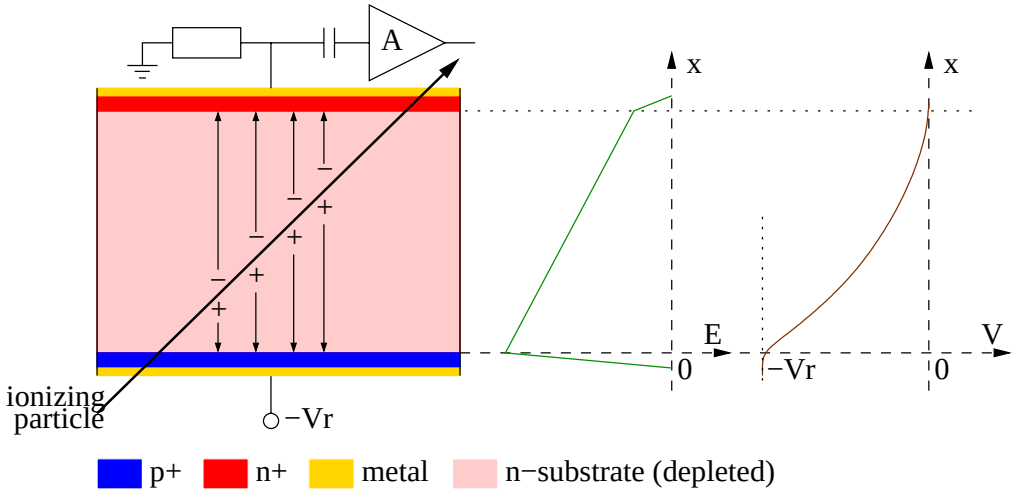


Figure 2.2: Reverse biased p^+-n junction, electrical field distribution and electrical potential profile across the junction.

2.1.2 Sideward depletion

In 1983 Gatti and Rehak [Gat84] proposed a new detector scheme based on sideward depletion. The principle of this scheme is explained in Figure 2.3. The structure shown here consists of two p^+-n junctions sharing the same n-substrate. The substrate is contacted to ground by means of an n^+-implantation. If equal reverse voltages V_u and V_d are applied to the upper and the lower p^+-contact respectively, the depletion of the n-substrate starts from both sides (see Figure 2.3a). Increasing the voltage values, the two depletion zones touch each other in the middle of the substrate. The electrical potential seen by electrons has a minimum in this position (see Figure 2.3b). If $V_u \neq V_d$, the potential minimum is shifted toward the node with the higher potential. This is the situation depicted in Figure 2.3c.

The electrical potential distribution $V(x)$ can be determined from the one-dimensional Poisson equation:

$$\frac{d^2V(x)}{dx^2} = -\frac{\rho}{\epsilon_s} \tag{2.7}$$

where $\rho = q \cdot N_D$ is the charge density in the depleted substrate. Assume that the entire substrate of thickness d is depleted (Figure 2.3b and 2.3c). The solution of the Poisson equation 2.7 with the boundary conditions $V(0) = V_u < 0$, $V(d) = V_d < 0$ is given by:

$$V(x) = \frac{\rho}{\epsilon_s}x(d-x) + \frac{x}{d}(V_d - V_u) + V_u \tag{2.8}$$

The position of the potential minimum (the solution of $dV/dx = 0$) and the potential value at this point are:

$$x_{min} = \frac{d}{2} + \frac{\epsilon_s}{\rho} \cdot \frac{V_d - V_u}{d}; \qquad V(x_{min}) = \frac{V_d + V_u}{2} + \frac{V_o}{4}\left[1 + \frac{(V_d - V_u)^2}{V_o^2}\right] \tag{2.9}$$

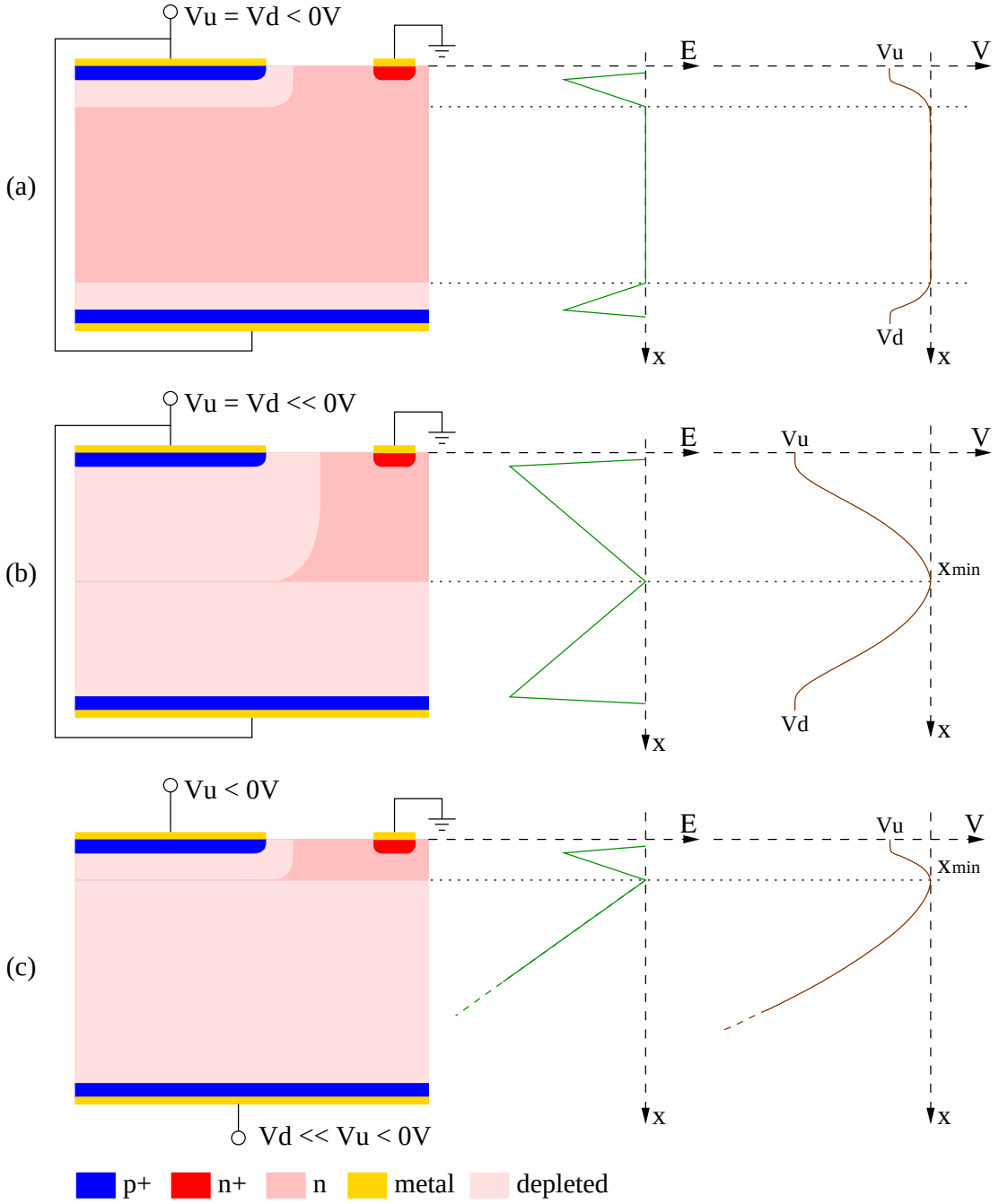


Figure 2.3: Principle of the sidewards depletion. Electrical field and potential distribution for various applied voltages.

where $V_o = d^2\rho/(2\epsilon_s)$. Recalling the equation 2.6, V_o is the voltage necessary to deplete the whole substrate if acting only from one side of the structure (i.e. V_u or V_d are set to zero).

For symmetrical boundary conditions $V_u = V_d$ the position of the potential minimum

is $x_{min} = d/2$. Imposing $V(x_{min}) = 0$, one obtains from equation 2.9:

$$V_u = V_d = -\frac{V_o}{4} \tag{2.10}$$

The above expression tells us that if the structure is depleted from both sides, the reverse voltage needed for a full depletion of the substrate is a quarter of the value which is needed if depleting from one side only.

For non-symmetrical boundary conditions ($V_u \neq V_d$) the position of the potential minimum x_{min} can be chosen at any point within the detector by choosing the appropriate values of V_u and V_d.

Consider now the structure in Figure 2.4a. The homogeneous p^+-regions from the lateral sides of the substrate are replaced by a pattern of p^+ implants, each one connected to a separate voltage. Figure 2.4b shows the simulated two-dimensional potential distribution with the given applied voltages. The potential distribution in the y-direction has a local minimum whose position varies in the x-direction from the center of the substrate to zero with decreasing x. The value of this potential minimum also decreases as one

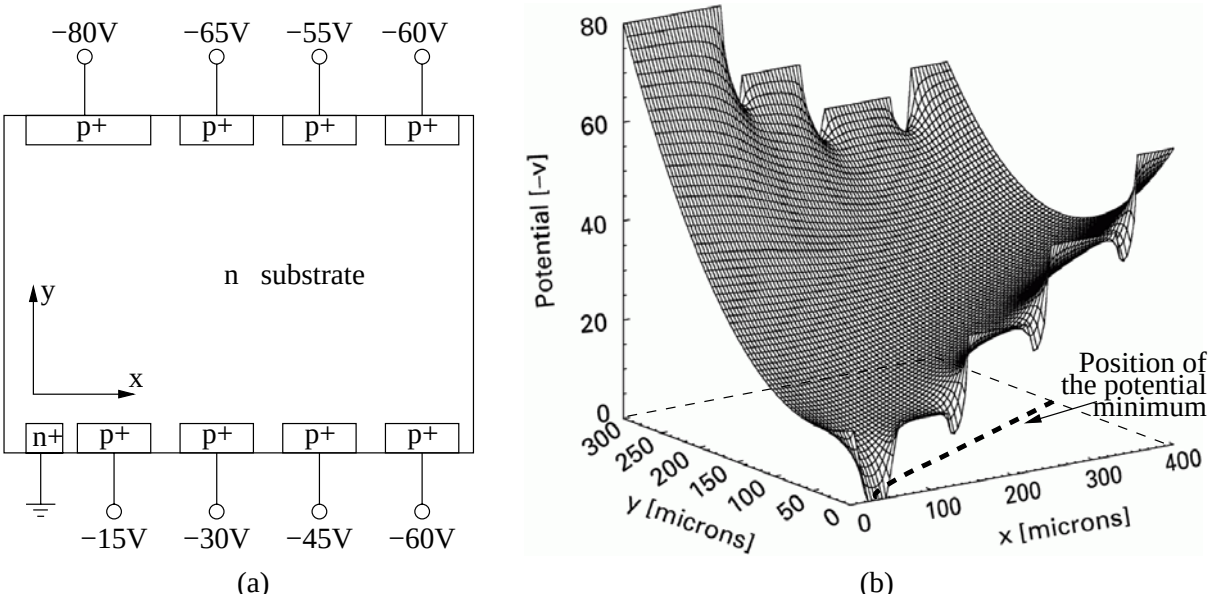


Figure 2.4: (a) Semiconductor drift chamber. (b) Potential distribution inside the detector [Str00].

approaches the n^+-contact. The signal electrons generated in the detector substrate drift initially to the local potential minima and from there to the n^+-node (the readout node). This depletion scheme combines the advantages of a large depleted substrate, i.e. large sensitive area, with the small capacitance of the readout node, i.e. large Signal-to-Noise ratio.

The principle that was described above is used in the DEPFET detectors, but also for the silicon drift detectors (SDDs) [Lec01] and for the *pn*-CCD [Str95, Str00] detectors.

2.2 The JFET transistor

The signal charges from the detector have to be read and amplified by subsequent readout electronics. The first stage of such a readout circuit - the preamplifier - has usually in the input a Field-Effect-Transistor (FET) like MOSFET (Metall-Oxide-Semiconductor-FET) or JFET (Junction-FET).

The simplified structure of a p-channel JFET transistor is shown in Figure 2.5. The

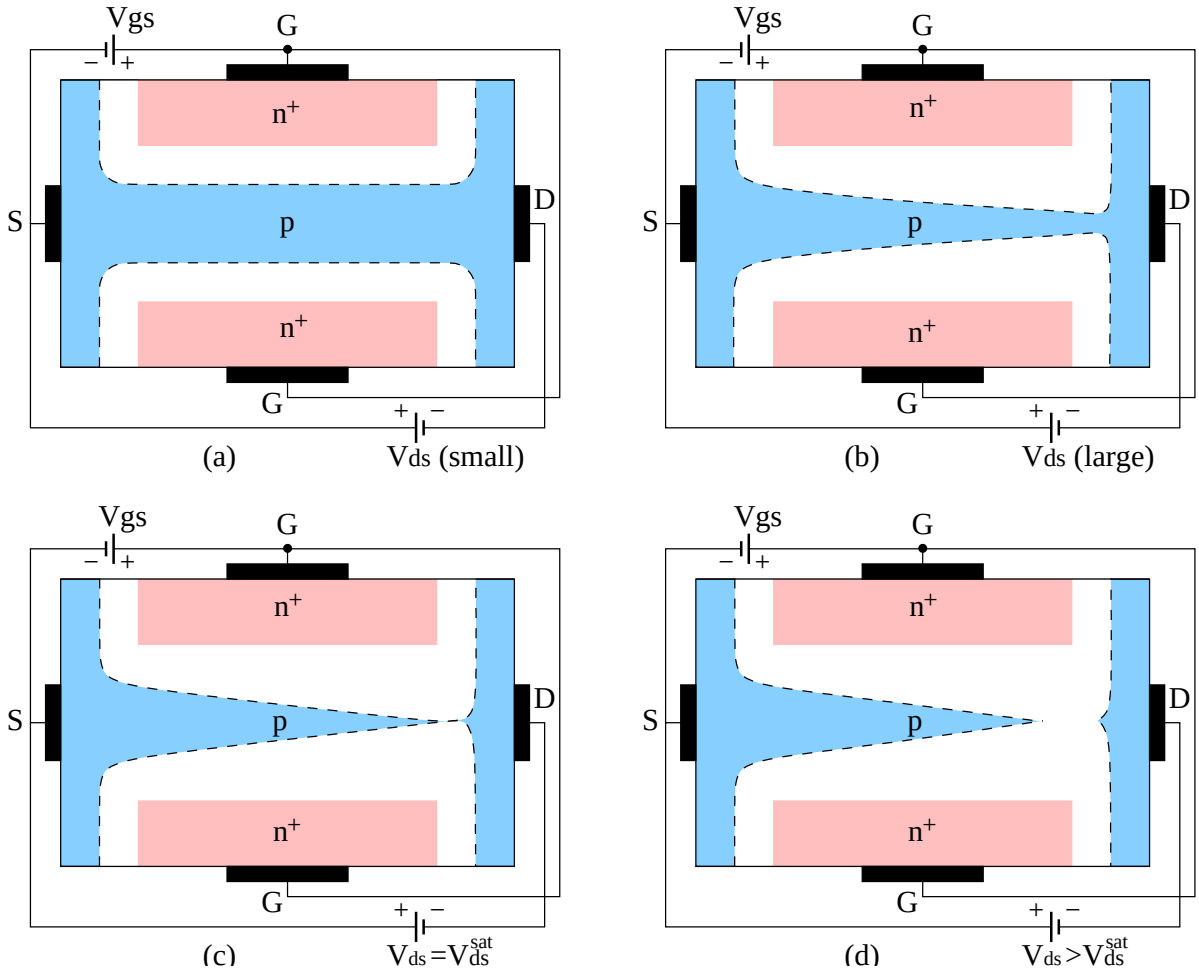


Figure 2.5: Operation of a p-channel JFET: (a) linear region; (b) non-linear region; (c) pinch-off region; (d) saturation region.

device consists of a p-type channel having n^+-type regions diffused on its lateral sides; these are the so-called transistor *gates* (G). The contacts at the ends of the transistor channel are called *source* (S) and *drain* (D). Although the device is symmetrical, for a p-channel JFET the drain node is negative with respect to the source node. For an n-channel device the drain is positive with respect to the source.

If a positive voltage is applied between the gate and the source contact, the gate-channel junctions are reverse biased. Their corresponding depletion zones get wider and the transistor channel becomes narrower. Assume now that a small voltage V_{ds} is applied

between source and drain (Figure 2.5a). The channel is almost of uniform width and the JFET simply operates as a linear resistor with the resistance value controlled by V_{gs}. The value of the drain-source current I_{ds} increases linearly with the drain-source voltage.

For larger values of V_{gs}, a special situation is reached when the entire channel is depleted. No current flows into the channel in this case. The value of V_{gs} at which this happens is called *pinch-off* voltage, denoted here by V_{po}.

Now consider the situation illustrated in Figure 2.5b. Here the gate-source voltage is kept constant at a value between 0 and V_{po} and V_{ds} increases. As we move along the channel from source to drain, the reverse bias voltage on the gate-channel junction increases and is highest at the drain. The channel acquires a tapered shape and the transistor characteristic I_{ds}- V_{ds} becomes non-linear (the channel resistance depends on V_{ds}).

Increasing further the value of V_{ds}, the reverse voltage on the gate-channel junction reaches the pinch-off value V_{po} at the drain node (see Figure 2.5c). The channel is pinched off at the drain and the channel current saturates. The corresponding drain-source voltage is called *saturation* voltage V_{ds}^{sat} and is given by $V_{ds}^{sat} = V_{po} - V_{gs}$. For values of V_{ds} larger than V_{ds}^{sat}, the pinch-off point moves toward the source (Figure 2.5d). The channel current increases slightly with increasing V_{ds} because of the finite resistance of the depletion region. This is the so-called Early effect.

One distinguishes three regions of operation for the JFET transistor:

a) Cutoff region: $V_{gs} \geq V_{po}$ - no current flows into the channel

b) Triode region: $0 \leq V_{gs} \leq V_{po}$ and $V_{ds} \leq V_{po} - V_{gs}$; I_{ds} is given by [Gray84]:

$$I_{ds} = G_o \left[V_{ds} - \frac{2}{3} \frac{(V_{gs} + V_{bi} + V_{ds})^{3/2} - (V_{gs} + V_{bi})^{3/2}}{(V_{po} + V_{bi})^{1/2}} \right] \tag{2.11}$$

c) Saturation region: $0 \leq V_{gs} \leq V_{po}$ and $V_{ds} \geq V_{po} - V_{gs}$; I_{ds} is given by [Gray84]:

$$I_{ds} = I_{ds}^{sat}(1 + \lambda V_{ds}); \qquad I_{ds}^{sat} = G_o \left[V_{po} - V_{gs} - \frac{2}{3} \frac{(V_{po} + V_{bi})^{3/2} - (V_{gs} + V_{bi})^{3/2}}{(V_{po} + V_{bi})^{1/2}} \right] \tag{2.12}$$

where V_{bi} is the built-in voltage of the gate-channel junction , λ is the inverse of the Early voltage $\lambda = 1/V_A$ and $G_o = aqN_A\mu_h W/L$, where a is the channel depth, W is the channel width, L is the channel length, N_A is the impurity concentration in the channel and μ_h is the hole mobility.

The current-voltage characteristics described by the above equations are plotted in Figure 2.6. The I_{ds}-V_{ds} characteristic is plotted in Figure 2.6a at different V_{gs} values. The triode and the saturation regions are separated by the black dash-dotted line. The dashed lines in the saturation region represent the constant saturation current, if the Early effect is neglected.

Figure 2.6b shows the saturation current I_{ds}^{sat} (given by the equation 2.12) plotted as a function of the gate-source voltage. I_{DSS} is the I_{ds}^{sat} value at $V_{gs} = 0$. Also plotted in the graph is a square law characteristic given by:

$$I_{ds}^{sat} = I_{DSS} \left(1 - \frac{V_{gs}}{V_{po}} \right)^2 \tag{2.13}$$

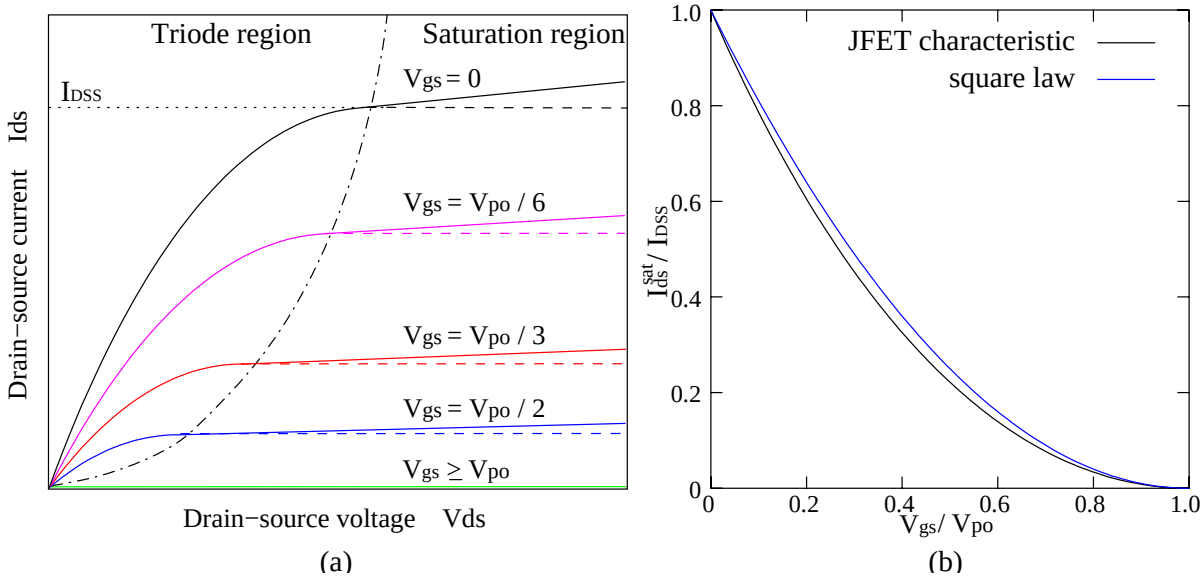


Figure 2.6: Current-voltage characteristics of the JFET: (a) I_{ds} *vs.* V_{ds}; (b) I_{ds}^{sat} *versus* V_{gs}.

The two curves agree quite well and the equation 2.13 is commonly used as an approximate expression of the transistor saturation current. Combining the equations 2.12 and 2.13, one obtains a simplified characteristic of the transistor in the saturation region:

$$I_{ds} = I_{DSS}\left(1 - \frac{V_{gs}}{V_{po}}\right)^2 (1 + \lambda V_{ds}) \tag{2.14}$$

The saturation region of the transistor is of most interest in electronics. A small voltage variation on the gate produces a large variation in the saturation current and the transistor behaves like a voltage-controlled current source. The input port of the current source is between gate and source, while the output port is between drain and source. There are two important parameters which characterize the performances of such a device: the *transconductance* and the *output impedance*.

The transconductance parameter denoted by g_m^{sat} is defined as $g_m^{sat} = \partial I_{ds}/\partial V_{gs}$. Using the square law approximation from equation 2.14 and neglecting the Early effect, i.e $\lambda = 0$, the JFET transconductance is:

$$g_m^{sat} = -2\frac{I_{DSS}}{V_{po}}\left(1 - \frac{V_{gs}}{V_{po}}\right) = -2\frac{\sqrt{I_{DSS}}}{V_{po}}\sqrt{I_{ds}^{sat}} \tag{2.15}$$

and is plotted in Figure 2.7. Also plotted here is the transconductance determined from the exact characteristic described by the equation 2.12. The two curves are in good agreement except the region around $V_{gs} = 0$.

It can be seen from equation 2.15 that g_m^{sat} is linear with V_{gs} and intersects the V_{gs}-axis at V_{po}. In practice, this makes possible the accurate determination of the pinch off voltage.

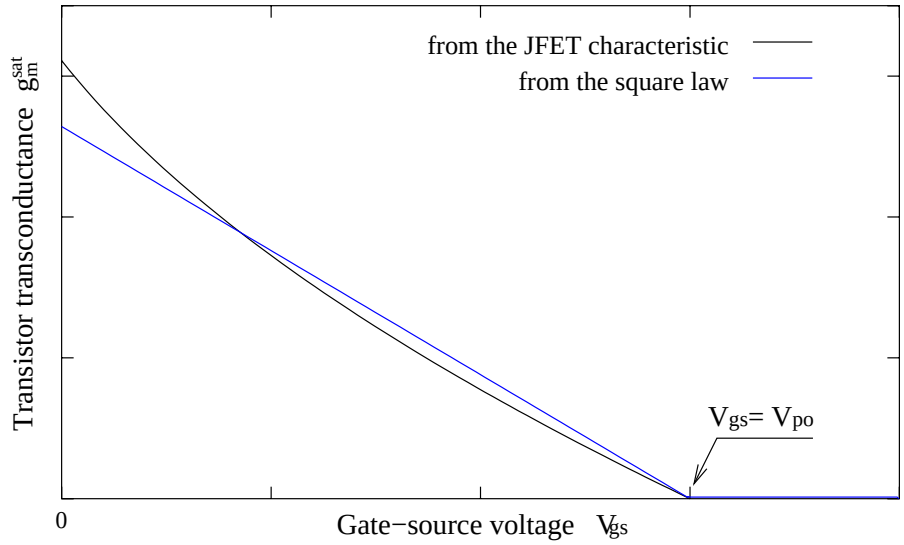


Figure 2.7: Transconductance of the JFET transistor in the saturation region.

The other important parameter - the output impedance r_o - is defined by $r_o = \partial V_{ds}/\partial I_{ds}$. Using the transfer characteristic from equation 2.14, the output impedance is:

$$r_o = \left[I_{DSS} \left(1 - \frac{V_{gs}}{V_{po}} \right)^2 \lambda \right]^{-1} \approx \frac{1}{\lambda I_{ds}} = \frac{V_A}{I_{ds}} \tag{2.16}$$

For large values of V_A (tens of volt) and values of I_{ds} of the order of hundreds of μA, the output impedance impedance is very large (hundreds of $k\Omega$). The impact of these two parameters on the JFET performances will be discussed in more details in the next chapter.

The fabrication of a JFET transistor makes use of a special technique called planar technology [Kem84], [Sed98]. Figure 2.8 shows such a JFET device realized in the planar process. The fabrication process begins with an n-type silicon substrate which is firstly passivated by thermal oxidation. A SiO_2 layer is thus formed on the top surface. Using photolithographic equipment and special etching techniques, windows are opened in the oxide layer to enable the doping of those regions with the desired doping profiles. The doping process can be performed by means of impurity diffusion and ion implantation. The later is preferred, as it can be performed at low temperature. Additionally, the impurity implantation profiles can be controlled very precisely, by controlling the energy and the dose of the impurity atoms. In order to obtain low ohmic contacts at source and drain, p^+-regions are formed on the transistor channel. For the external connections, a metal (e.g. Al or Au) layer is evaporated onto the corresponding contact regions.

MOSFET transistors can also be used in the input stage of the detector pre-amplifier. The essential difference is that in a MOSFET the current flows at the semiconductor-oxide interface, while in a JFET the current flows within the semiconductor substrate. As the number of the trapping centers is much larger at the semiconductor surface, the MOSFET has a considerably larger "*1/f*" noise than the JFET transistor. In high energy

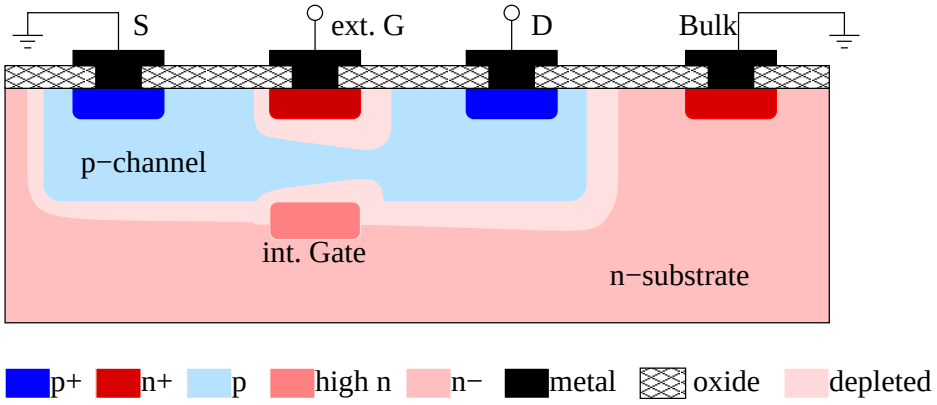


Figure 2.8: Realization of a JFET with the planar technology.

application, the semiconductor-oxide interface of the MOSFET can be easily damaged by ionizing particles, in contrast to the JFET transistor which has a better radiation hardness.

2.3 JFET integration in the DEPFET detector

The charge signals from a semiconductor detector have to be further amplified and processed by a readout system. The basic idea in realizing a DEPFET detector is to integrate the first component (usually a JFET or a MOSFET transistor) of such a circuit directly on the detector substrate. The integration scheme is explained in Figure 2.9 The readout

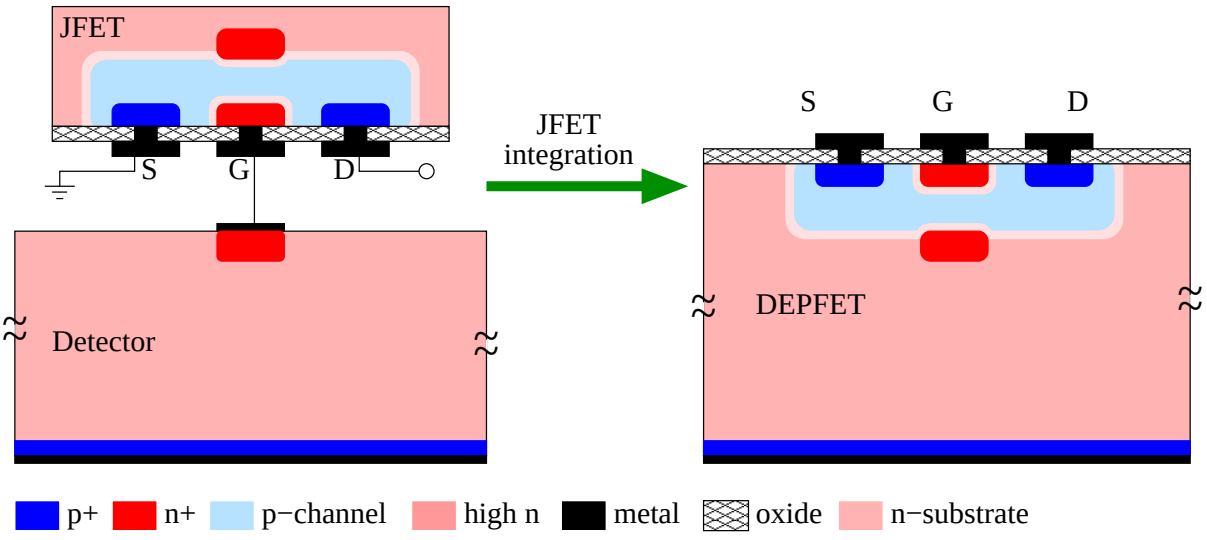


Figure 2.9: The JFET transistor integration in the DEPFET detector.

node of the detector merges with the internal gate of a *p*-channel JFET transistor, as they have the same type of impurity implantation. Combining these two structures with

the principle of sideward depletion, one obtains the DEPFET detector which is an active detector, i.e. detector with integrated pre-amplifier.

The structure of a depleted DEPFET detector is shown schematically in Figure 2.10. The device has a cylindrical symmetry with respect to the vertical axis at the JFET source. The additional p^+-type guard rings (R_1, R_2) formed around the JFET channel are used to shape the electrical potential in the detector substrate. A potential minimum for electrons is created underneath the transistor channel (recall the sideward depletion scheme explained in the section 3.1). This potential minimum is locally confined to the internal gate region, due to the its higher n-concentration.

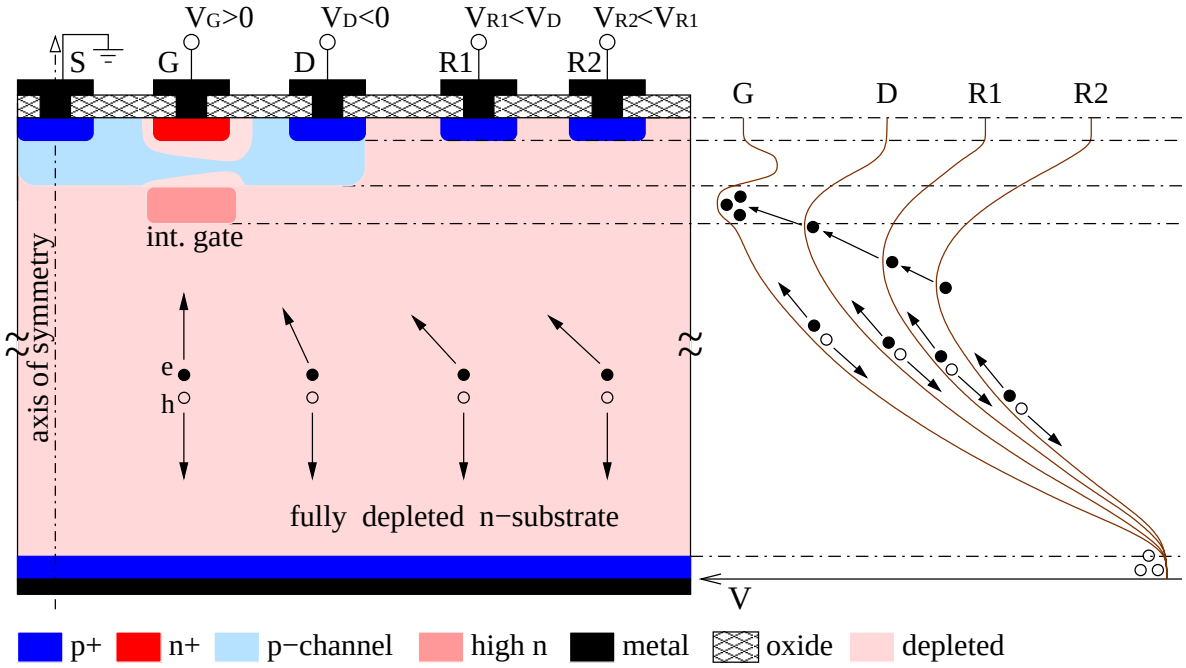


Figure 2.10: The working principle of the DEPFET detector; electrical potential distribution across the detector.

An ionizing particle which hits the detector produces electron-hole pairs in the depleted substrate . The holes drift to the most negative node (the p^+-contact on the back side), while the electrons drift to the potential minimum formed at the internal gate. They induce a negative voltage change on the small equivalent capacitance of the internal gate and the transistor current increases. This current change is proportional to the number of electrons in the internal gate and is further amplified and processed by an appropriate readout circuit.

2.4 Clear mechanism of the DEPFET detector

The internal gate of the DEPFET collects not only the signal electrons generated by ionizing particles, but also the electrons that are thermically generated in the depleted

substrate. To prevent the over-filling with electrons at the potential minimum and therefore the detector becoming insensitive, a "clear" mechanism has to be employed. There are two methods of removing the collected charges from the DEPFET internal gate: pulsed clear mechanism and continuous clear mechanism.

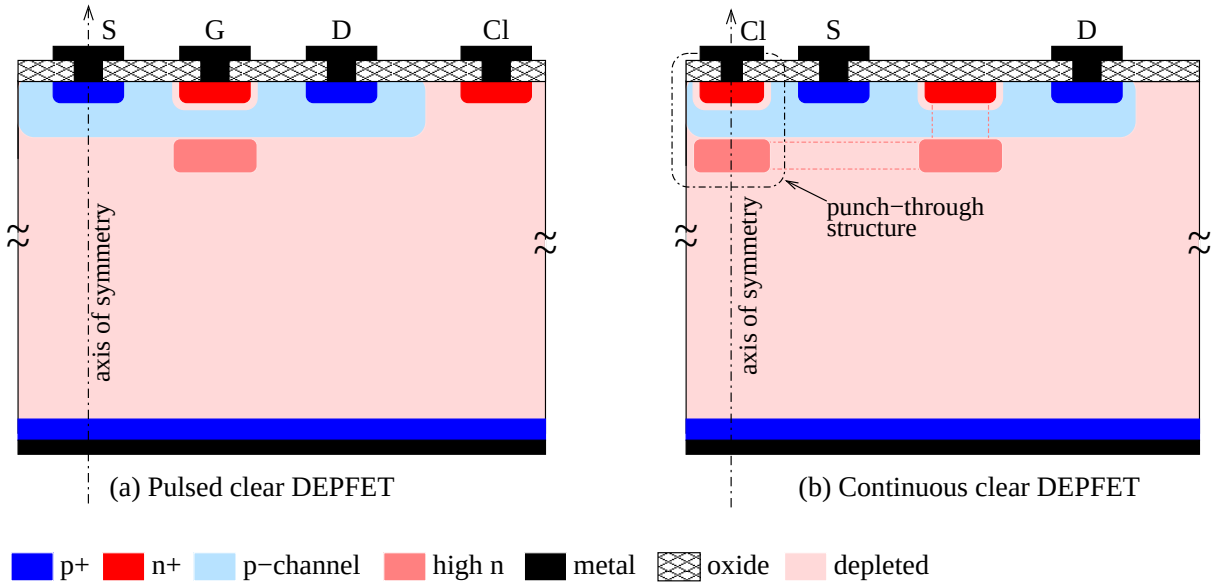


Figure 2.11: The clear mechanism of the DEPFET detector: (a) pulsed clear DEPFET and (b) continuous clear DEPFET.

In the case of the pulsed clear DEPFET (see Figure 2.11a), an n^+-region is implanted on the detector, outside the guard ring structure (not shown here). A positive voltage pulse is applied periodically to the clear contact (Cl) and the electrons from the internal gate drift to the contact within the time duration of the applied pulse. The dead time introduced by applying the clear pulse is much shorter than the detector sensitive time. In normal operation, electrons are collected at the internal gate irrespective of whether the transistor is switched on or off. The collected signal charge is nevertheless detected when the JFET is switched on (at regular time intervals). The pulsed clear DEPFET is thus an integrating detector device.

In the case of the continuous clear DEPFET (Figure 2.11b) an n^+-implant region is formed on the transistor channel near the source. This region forms together with the p-region of the transistor channel and the high n implant of the internal gate a so-called *punch-through* structure. The properties of the structure are discussed in details in the next sub-section. When a constant positive voltage is applied to the clear contact, a small steady current flows through the structure and removes continuously the electrons collected at the internal gate.

In the devices which were used in the present thesis, the transistor gates are connected by a vertical opening in the channel implantation. This leads to an increased transconductance, as the transistor current is controlled from both sides of the channel. Furthermore, since the internal gate voltage can be controlled by the clear voltage (more about this in

the following sub-section), the upper gate needs no external connection; its length can be reduced to the photolithographic limit, thus reducing the gate capacitance and increasing the signal-to-noise ration.

In contrast to the pulsed clear DEPFET, the continuous clear DEPFET is a counting detector. This means that the detector is continuously sensitive and responds to any charge pulse generated in the detector substrate. In a pixel matrix configuration, all the DEPFET cells have to be read individually. This can be done by employing a special connection technology called *bump bonding*. Each pixel in the detector matrix is connected to the corresponding pixel in the readout electronics matrix through a metal bump. A continuous clear DEPFET matrix is thus appropriate for applications with low counting rates.

2.4.1 The n^+-p-n punch-through clear structure

The working principle of the punch-through structure [Sze81] is described in Figure 2.12 The structure consists of two semiconductor junctions n^+-p and p-n, sharing the same p-region of width W. To illustrate in a simple way how the structure works, it is assumed that the n-region is connected to ground (this is not the case in the real operation of the DEPFET detector).

The potential distribution at equilibrium is shown in Figure 2.12a. The electrons from the n-region see a potential barrier of height V_b^o and cannot enter the p-region. When a positive voltage V_{cl} is applied, the n^+-p junction is reverse biased. The current which flows through the structure is practically the leakage current of the reverse bias junction. This current is mainly due to the generation-recombination processes in the depletion zone and is proportional to the depletion width W_1 [Sze81]:

$$J_{g-r} = \frac{q \cdot n_i}{\tau_e} W_1 \propto \sqrt{V_{cl} + V_b^o} \tag{2.17}$$

where n_i is the intrinsic carrier concentration and τ_e is the effective lifetime.

Increasing the value of V_{cl}, the depletion zone of the p^+-n junction widens. At a voltage value called *reach-through* voltage V_{rt}, the depletion regions of both junctions touch each other (see Figure 2.12b). If V_{cl} is increased beyond the reach-through value (Figure 2.12c), the potential barrier V_b decreases and the p-n junction becomes forward biased. Electrons from the n-region injected into the p-region by means of thermionic emission, drift very fast to the n^+-region due to the electrical field distribution. The current increases exponentially with the applied voltage and is given by [Chu72]:

$$J_{n \to p} = A^* \cdot T^2 exp\left[-\frac{q(V_{fb} - V_{cl})^2}{4kT \cdot V_{fb}}\right] \tag{2.18}$$

where A^* is the Richardson constant for electrons and T is the absolute temperature. The voltage V_{fb} is called *flat-band* voltage and is the value of the applied voltage at which the potential barrier V_b vanishes completely (Figure 2.12d). The expression of V_{fb} is given by (see equation 2.6):

$$V_{fb} = \frac{qN_A}{2\epsilon_s} W^2 \tag{2.19}$$

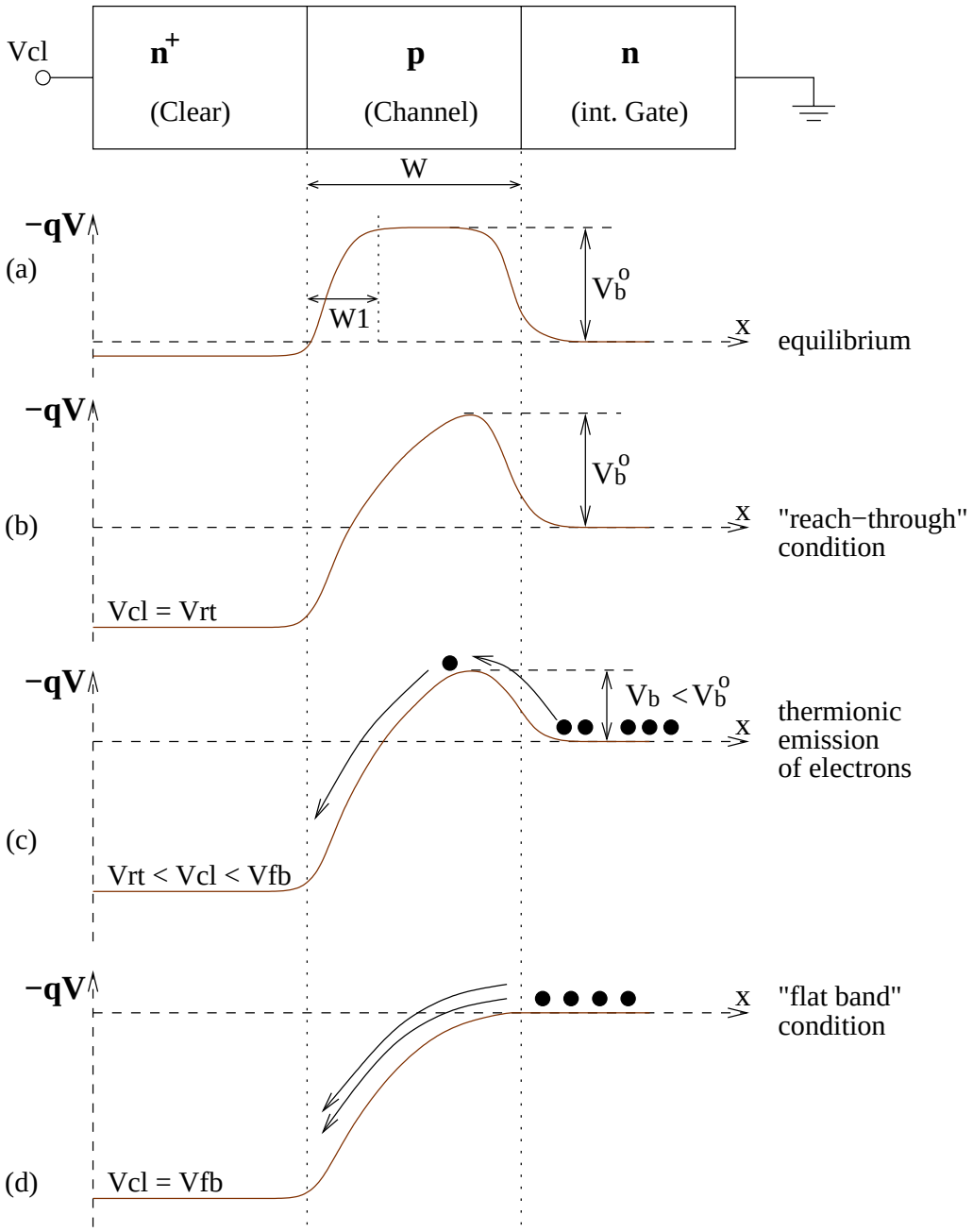


Figure 2.12: The punch-through structure. Potential distribution across the structure at (a) equilibrium, (b) reach-through condition, (c) thermionic emission of electrons and (d) flat-band condition.

where W is the width of the p-region and N_A is the impurity concentration in the p-region.

If the injected current is sufficiently high such that the injected carrier density is comparable to the ionized-impurity density N_A, the mobile charge carriers influence the field distribution in the drift region. This is the so-called *space-charge-limit* effect. The

current density saturates to its asymptotical limit given by [Chu72]:

$$J_s = qN_A v_s \frac{V}{V_{fb}} \tag{2.20}$$

where v_s is the scattering-limited velocity.

The current-voltage characteristic described by the equations 2.17, 2.18 and 2.20 are plotted in Figure 2.13a. One can see the three operation regions that were discussed above: the generation-recombination current at $V_{cl} < V_{rt}$, the exponential increase of the thermionic emission current for $V_{cl} > V_{rt}$ and the space-charge-limit effect at large values of the current density.

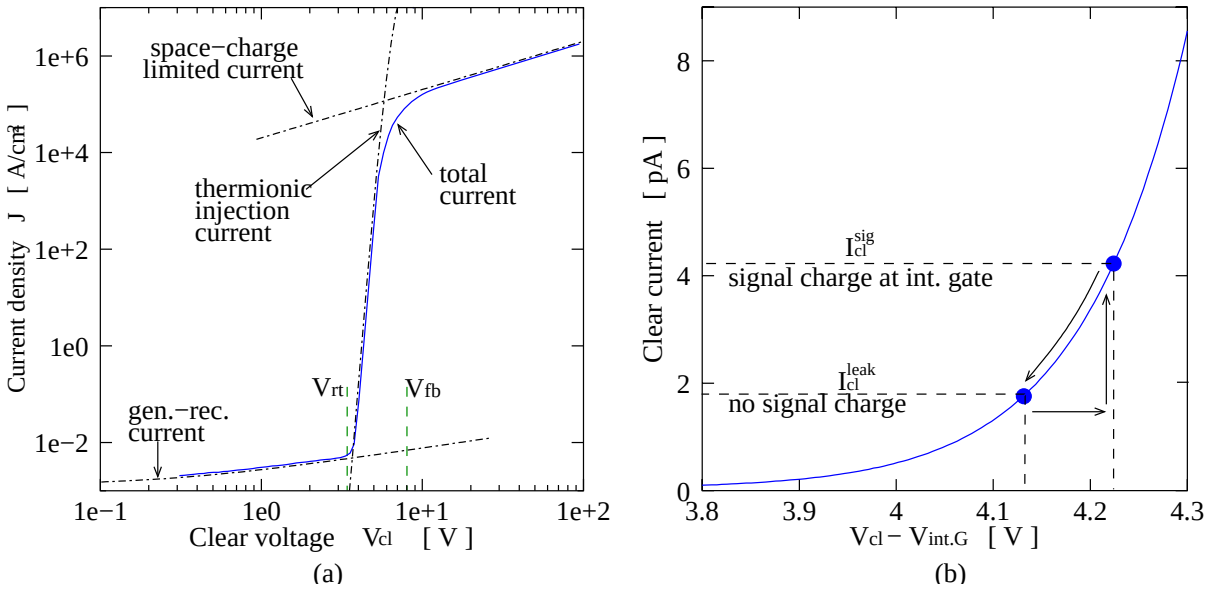


Figure 2.13: (a) Current-voltage characteristic of the punch-through structure; (b) same as (a) but in linear scale.

Figure 2.13b explains the operation of the punch-through structure when used for the DEPFET clear mechanism. The voltage on the x-axis is the now difference between the clear potential and the internal gate potential, as the high n-region of the DEPFET internal gate is not connected to ground. The DEPFET substrate is depleted and the current that flows through the structure is the leakage current of the depleted substrate I_{cl}^{leak}. Since this current is very low (order of pA), only a narrow region (around the reach-through point) of the current-voltage curve in Figure 2.13a will characterize the DEPFET clear mechanism.

Assume first that no signal charge is generated in the detector substrate. The constant leakage current I_{cl}^{leak} removes the electrons that are thermically generated in the depleted substrate. The potential difference between clear and internal gate will adjust itself to a value given by the current-voltage characteristic in Figure 2.13b. A change in the clear voltage is then automatically followed by the same change in the internal gate voltage. This is the way in which the gate potential of the JFET transistor can be controlled via the clear contact.

If an ionizing particle hits the detector, the generated signal electrons are collected at the internal gate. The gate potential becomes more negative, and correspondingly, the clear current increases on the $I-V$ characteristic to the value I_{cl}^{sig}. This current starts to empty the internal gate at a higher rate (proportional to the signal current). As the electrons progressively leave the internal gate, its potential returns slowly to the initial value and the clear current decreases towards I_{cl}^{leak}. The device has returned now to its operation point.

2.5 Description of the investigated DEPFET devices

The continuous clear DEPFET devices that are investigated within this work were fabricated at the Semiconductor Laboratory of Max Plank Institute in Garching [SEM03]. The structures are fabricated in planar technology [Kem84] on a high resistance silicon n-substrate. We investigate here four different versions of DEPFET detectors which are realized as single pixel structures on a silicon substrate. They are denoted by Type-I, -II, -III and -IV.

The layout of the Type-I DEPFET is shown in Figure 2.14. The structure consists of three guard rings of hexagonal shape formed around a p-channel JFET transistor also of hexagonal shape. The clear contact is in the center of the structure. The two openings in the channel implantation region connects the transistor gates. In order to be able to measure the transistor characteristics independently on the clear structure, the external gate is also contacted. A three-dimensional schematic view with a transverse cut through the device is shown in Figure 2.15. One can see here also the shape of the internal gate region (*deep-n* implantation) and the n^+-p-n punch-through structure under the clear contact.

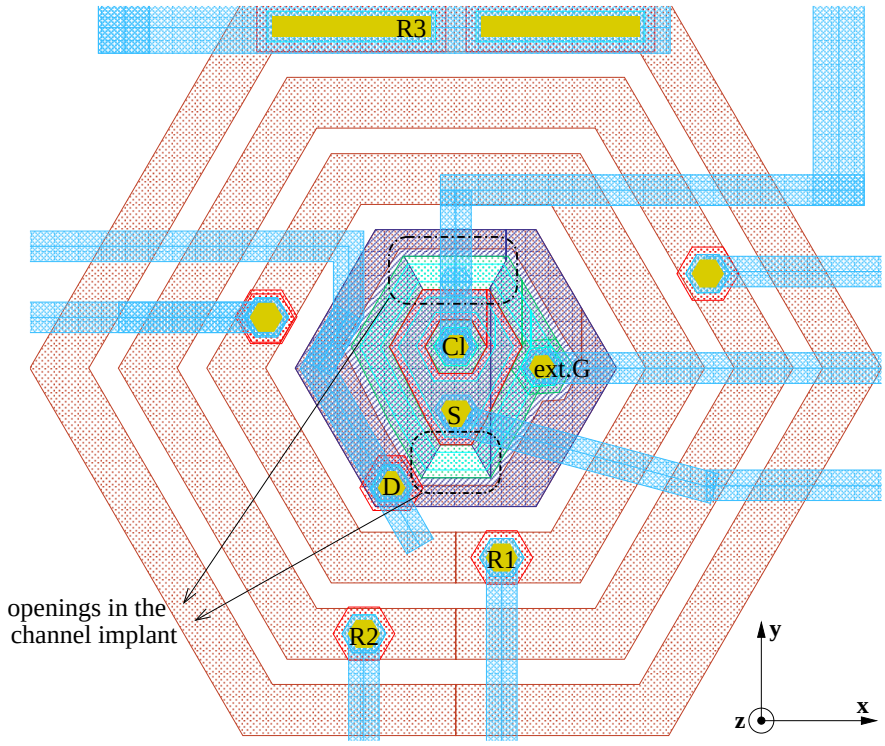


Figure 2.14: Layout of the continuous clear DEPFET of Type-I [SEM03].

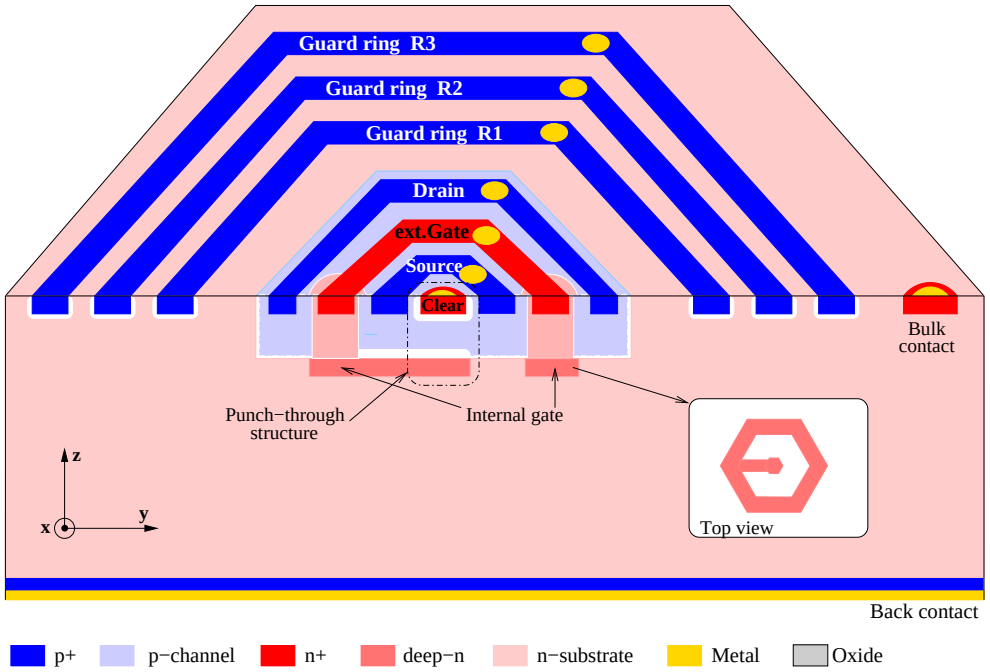


Figure 2.15: A transverse cut through the DEPFET detector of Type-I.

The DEPFET structure of Type-II is identical to the one of Type-I, except for the clear mechanism. Although it is still a continuous clear mechanism, it does not employ a punch-through structure, but an n-channel MOSFET structure operated in the subthreshold region. Figure 2.16 shows a transverse cut through the DEPFET structure. For simplicity, only one guard ring is drawn here. The n-MOSFET structure which is used for the clear mechanism consists of the n^+ clear implant (the MOSFET drain), the external gate $n+$ implant (the MOSFET source) and the p implant of the JFET channel as the MOSFET substrate (the p^+ implantation of the JFET source is missing in the region underneath the MOSFET). The metal layer which connects the clear contact is also used for the gate of the MOSFET. The structure works therefore as transistor in the diode configuration.

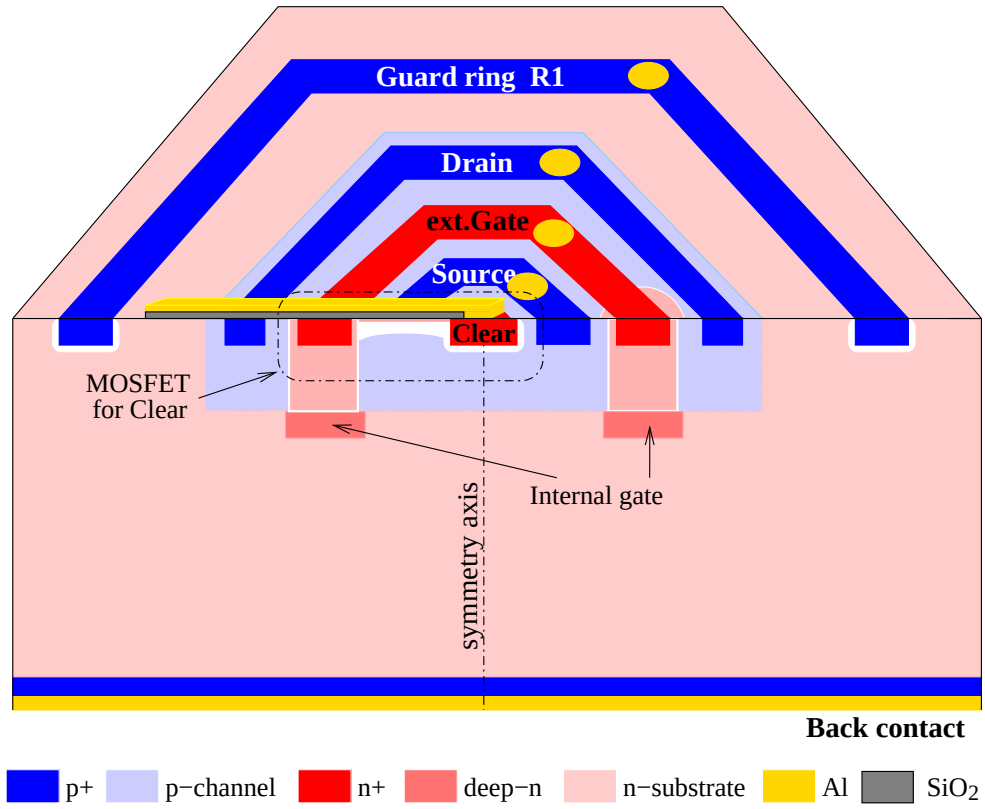


Figure 2.16: A transverse cut through the DEPFET detector of Type-I.

Like in the case of the punch-through structure, the clear current flowing through the MOSFET structure is the detector leakage current. At these current values, the current-voltage characteristic is exponential [Alle02] (the MOSFET is in the sub-threshold region). The internal gate voltage can be controlled via the clear voltage in the same way as for the DEPFET detector with the punch-through structure for clear.

The DEPFET of Type-III and -IV have the same clear mechanism as Type-I and -II, respectively, but the JFET is slightly different. To reduce the dimensions of the JFET transistor and therefore the internal gate capacity, the source, gate and drain implants are adjacent to each other. Figure 2.17 shows a similar cut through the DEPFET devices of last two types, the clear structure missing in the drawing.

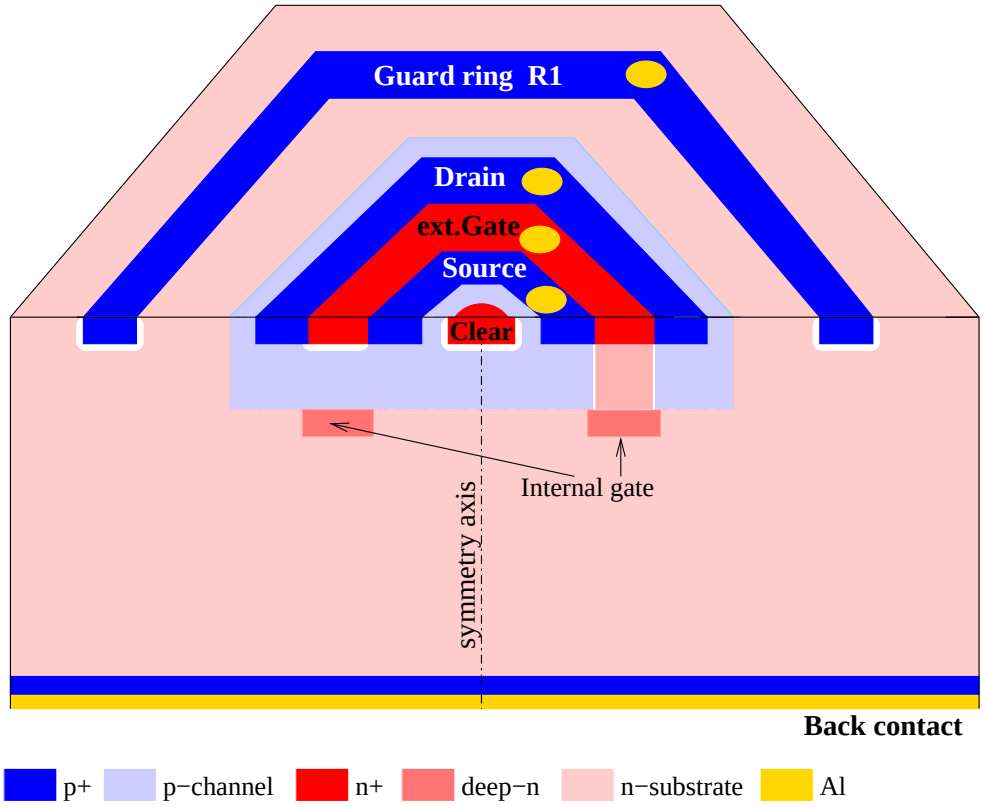


Figure 2.17: A transverse cut through the DEPFET detector of Type-III and IV.

Since no channel region is left between source and gate or between gate and drain, the JFET channel current flows deep in the channel and therefore, avoids the trapping centers which are present at the surface. The *"1/f"* noise component can be reduced in this way [Lut99].

Chapter 3

Static measurements of the DEPFET detectors

This chapter presents the static characteristics measured for the four types of DEPFET structures. The measurements include the transistor characteristics, the characteristics of the clear structure, the depletion characteristics of the detector substrate and again the characteristics of the JFET, but measured with the detector substrate depleted.

3.1 Static characteristics of the JFET transistor

The static characteristics of the JFET transistor are measured at first independently on the detector substrate. The JFET source is connected to ground, external voltages are applied to the external gate and drain contacts and all the other DEPFET nodes (back contact, substrate, guard rings and clear contacts) are left unconnected.

3.1.1 Static characteristics of the JFET transistor of DEPFET Type-I and II

The I_{ds}-V_{ds} characteristics of the JFET transistor from the first two types of DEPFET are plotted in Figure 3.1. The drain-source current I_{ds} is measured as a function of the drain-source voltage V_{ds} for different values of the gate-source voltage V_{gs}. One can see the linear increase of the current at small values of V_{ds} and the saturation region for larger values of V_{ds} (compare to Figure 2.6 in chapter 2).

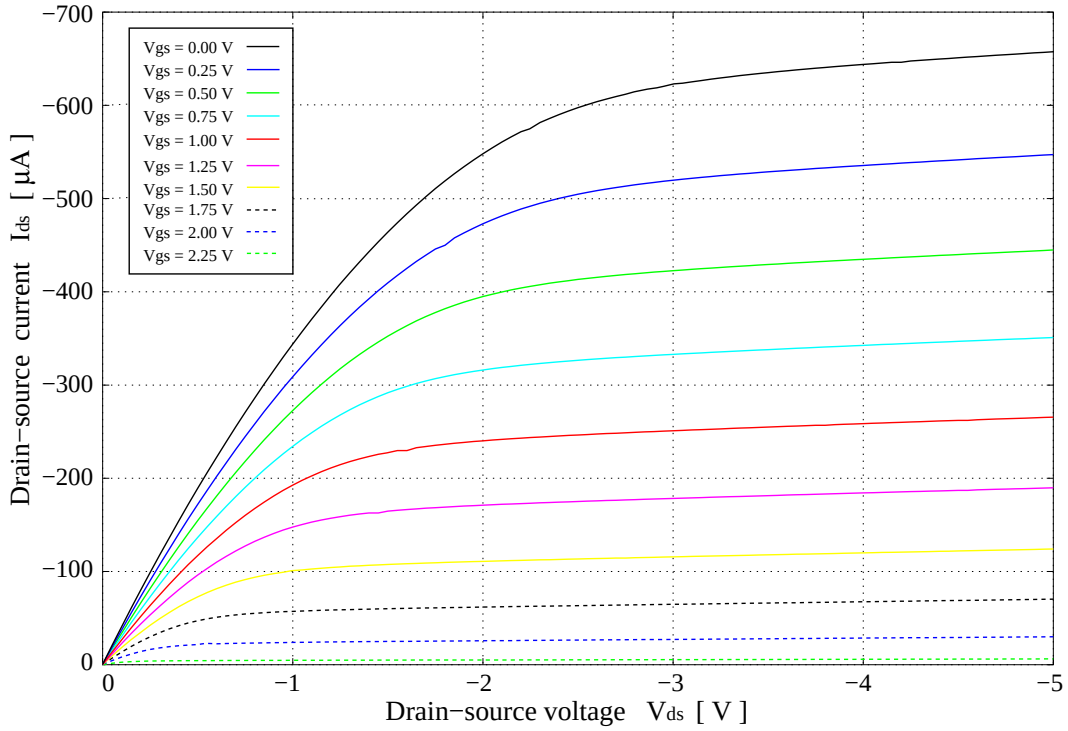


Figure 3.1: I_{ds}-V_{ds} characteristic of the JFET (DEPFET of Type-I and II).

With the drain-source voltage set to $V_{ds} = -3V$ (JFET in saturation), the drain-source current is measured with respect to the gate-source voltage. The characteristic is plotted in Figure 3.2a. The JFET transconductance parameter g_m which is proportional

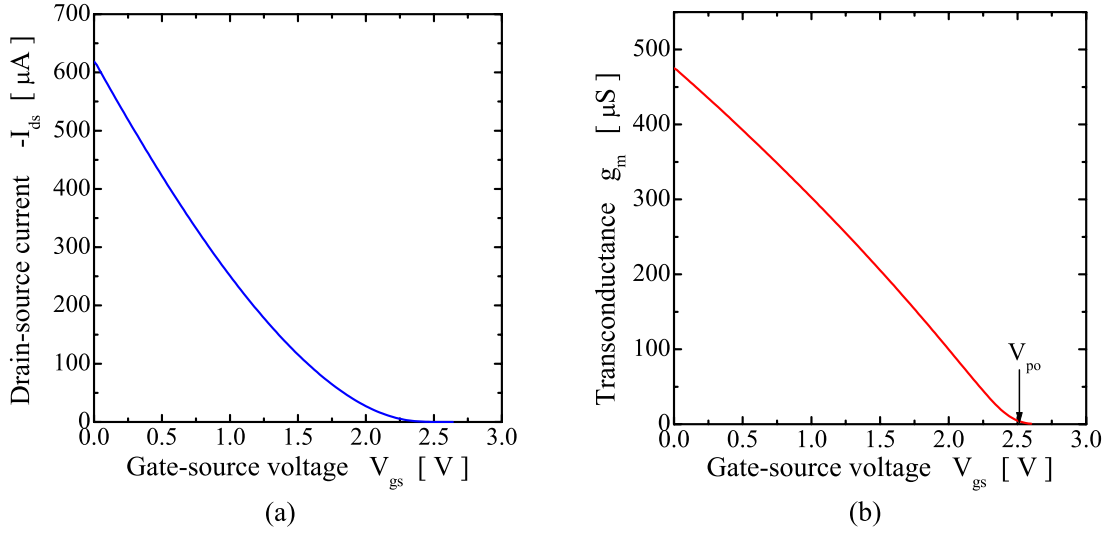


Figure 3.2: (a) I_{ds}-V_{gs} characteristic; (b) JFET transconductance g_m.

to $\sqrt{I_{ds}}$ (see the last part of equation 2.15) is plotted in Figure 3.2b. It can be seen that g_m varies almost linearly with V_{gs} and the value of the pinch-off voltage V_{po} (at which g_m intersects the V_{gs}-axis) is about 2.5 V.

3.1.2 Static characteristics of the JFET transistor of DEPFET Type-III and IV

The I_{ds}-V_{ds} characteristic of the JFET transistor from the DEPFET Type-III and IV are plotted in Figure 3.3. Notice that at similar values of V_{gs}, the drain source current is

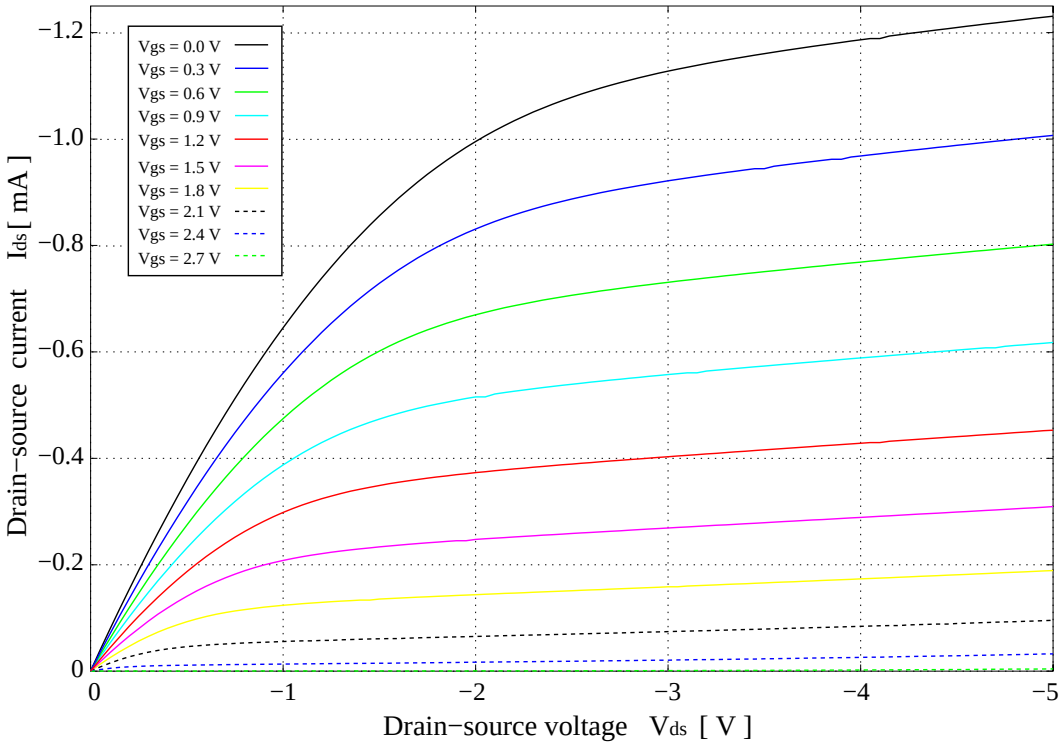


Figure 3.3: I_{ds}-V_{ds} characteristic of the JFET (DEPFET of Type-III and IV).

larger than in the JFET of the previous type. The design length of the JFET gate is the same for both transistors, but differences occur after the fabrication process. While in the previous JFET type, the effective gate length is larger than the design value due to the lateral diffusion, the effective gate length of the JFET of this type is smaller due to the vicinity of the p^+-implant regions of source and drain. Consequently, the parameter G_o from equation 2.12 is larger (G_o is inverse proportional to the channel length) and the drain-source current is larger.

The I_{ds}-V_{gs} characteristic (measured at $V_{ds} = -3V$) and the transistor transconductance are plotted in Figure 3.4. The pinch-off voltage is $V_{po} \approx 2.8V$.

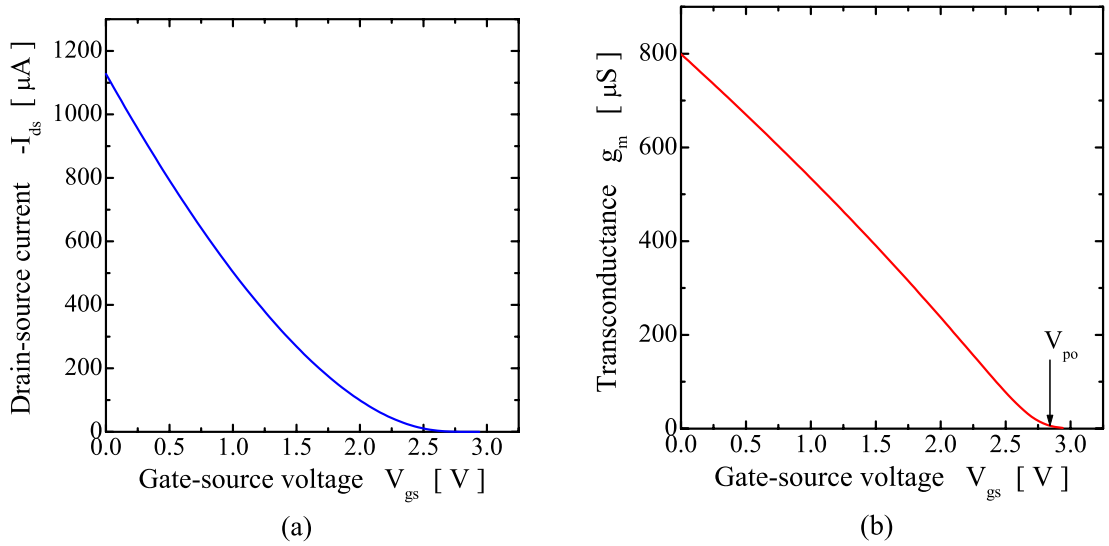


Figure 3.4: (a) I_{ds}-V_{gs} characteristic; (b) JFET transconductance g_m.

3.2 Static characteristics of the clear structures

The static characteristics of the two types of clear structures are measured also independently on the DEPFET substrate. Recall that the internal gate is connected to the external gate through the openings in the channel implant; the potential of the internal gate is set to ground by setting the external gate to ground. With all the other nodes left unconnected, an external voltage is applied to the clear contact and the clear current is measured.

Figure 3.5a shows the measured characteristic of the punch-through clear structure used in the DEPFET device of Type-I and III. The same curve is plotted at semi-logarithmic scale in Figure 3.5b. The reach-through voltage V_{rt} is about 4.8V and the current increases exponentially with the voltage for $V_{cl} \geq V_{rt}$. The space-charge-limited region where the current starts to saturate becomes visible at high current values. The dynamic resistance determined from the I_{cl}-V_{cl} curve as $R_d = dV_{cl}/dI_{cl}$ is plotted in the same graph (red curve). This resistance together with the internal gate equivalent capacitance defines the time constant of the clear mechanism. One can see that at small values of the clear current, the equivalent resistance has values in the range of hundreds of $G\Omega$. With the internal gate capacitance in the range of tens of fF, a clear time constant of the order of ms is achieved.

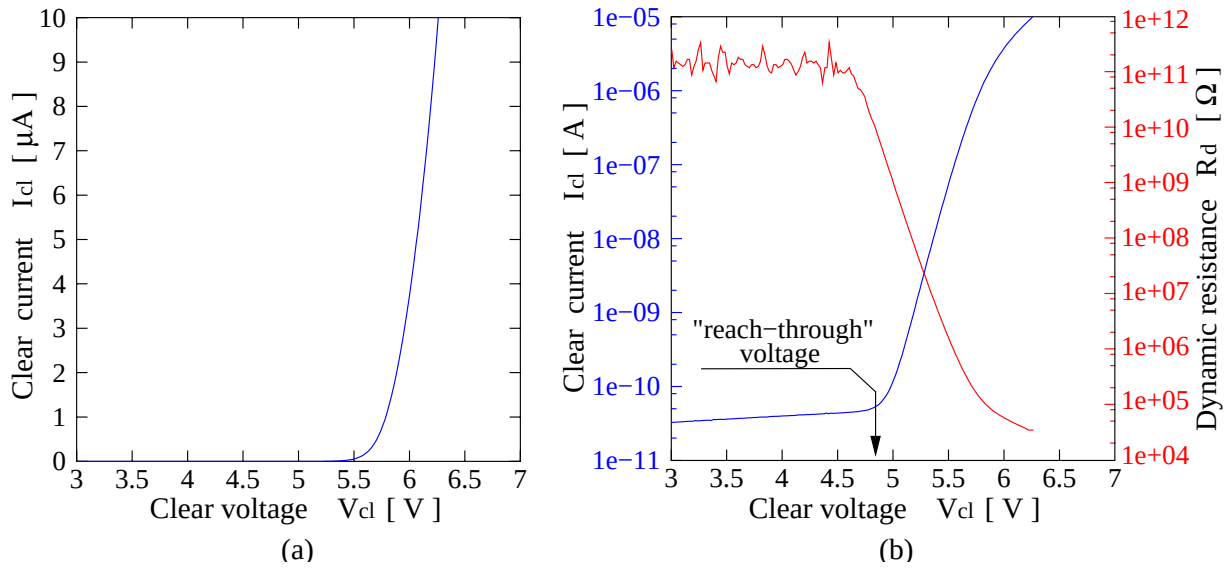


Figure 3.5: Static characteristic of the punch-through clear structure.

The static characteristics of the MOSFET clear structure used in the DEPFET device of Type-II and IV is plotted in Figure 3.6. It can be seen that the current increases

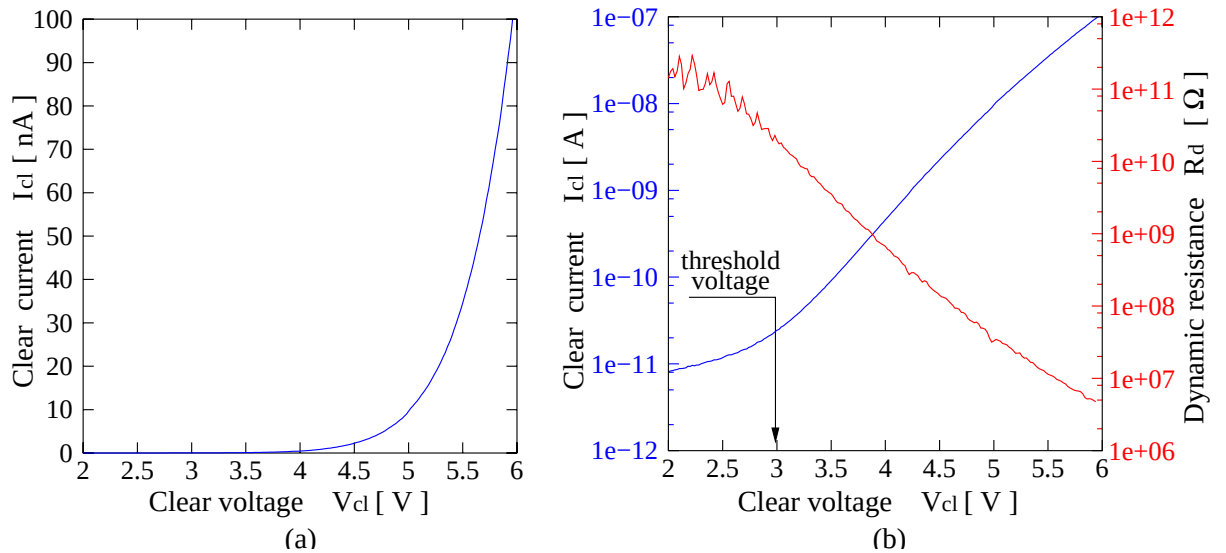


Figure 3.6: Static characteristic of the punch-through clear structure.

exponentially for voltage values above a threshold voltage of about 3V. The dynamic resistance plotted in Figure 3.6 has similar values as in the case of the punch-through structure.

3.3 Depletion characteristics of the DEPFET substrate

With the detector substrate connected to ground and all the other nodes left floating, a reverse voltage is applied to the back contact (p^+-implant on the back side) in order to deplete the detector substrate. The leakage current of the depleted substrate is measured versus the applied voltage and is plotted in Figure 3.7 (blue curve). If a p^+ guard ring

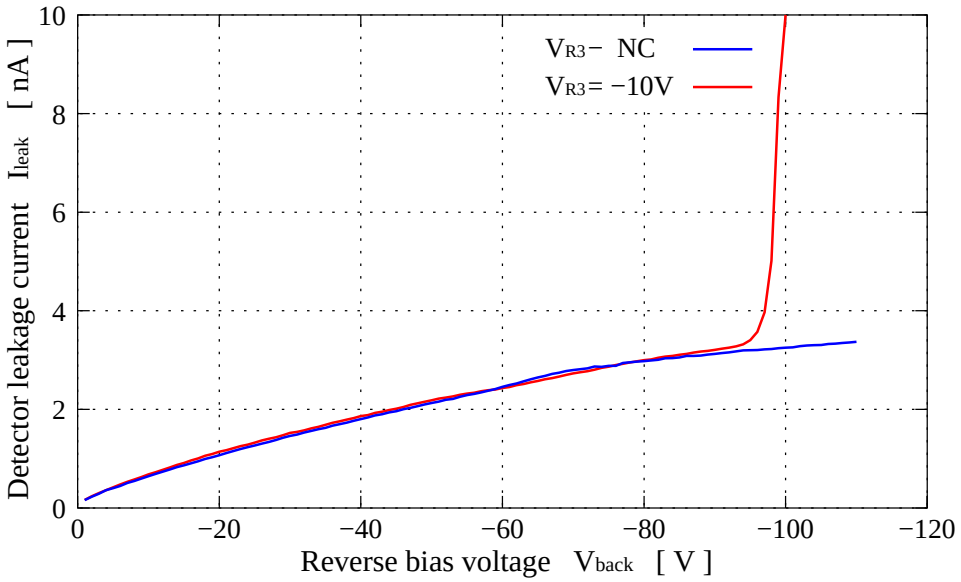


Figure 3.7: Detector leakage current.

(e.g. R3) on the top side is connected to a fixed potential (e.g. -10V), a p^+-n-p^+ punch-through structure is created between the p^+ guard ring, the n-substrate and the p^+ region on the back side. For reverse voltage values larger than the reach-through voltage of the structure, the current increases exponentially with the voltage (the red curve in Figure 3.7). Care must be therefore taken that the voltage difference between the p^+ guard rings on the top side and the p^+ region on the back side of the DEPFET is lower than the reach-through value. This is found to be $\approx -85V$.

An indirect method of determining the value of the reverse voltage at which the entire substrate is depleted, is to measure the resistance between two n^+ substrate contacts on the top side as a function of the applied reverse voltage. When the reverse voltage approaches the value that is needed for full depletion, the resistance between the substrate contacts increases very strong with the voltage. Applying a small voltage between the contacts, the current which flows between them decreases to zero at full depletion.

Figure 3.8 shows the current between two substrate contacts (with a voltage difference of 0.2 V) measured as a function of the reverse voltage applied on the back side. It can be seen that the current decreases to zero at a depletion voltage value of $\approx -86V$ at which the substrate is fully depleted.

In the later operation of the DEPFET, the guard rings are also connected to negative

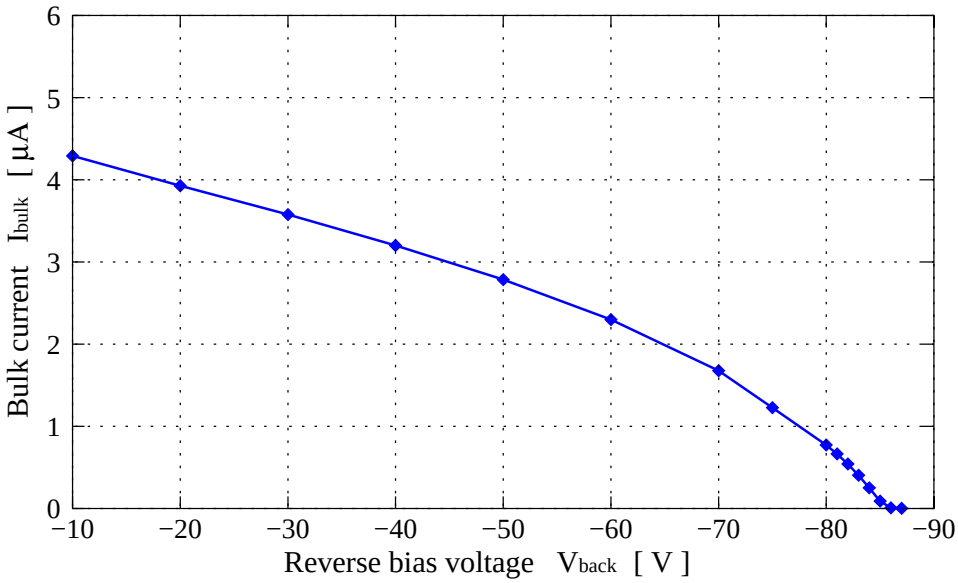


Figure 3.8: Substrate current versus the reverse bias voltage.

voltages. Since the detector substrate is depleted from both sides, the value of the reverse voltage necessary to deplete the whole substrate is actually smaller than the value determined here (recall the sideward depletion scheme).

3.4 JFET characteristics with the substrate depleted

The static characteristics of the JFET transistors were measured again with the detector substrate depleted. The external gate of the JFET is left unconnected and the internal gate voltage is controlled via the clear structure. The depletion voltage on the back side is set to $V_{back} = -80V$, the guard rings potentials are set to $V_{R1} = -10V$, $V_{R2} = -17V$ and $V_{R3} = -25V$ and the substrate contacts outside the guard rings are set to ground. With the transistor in saturation ($V_{ds} = -3V$), the drain-source current is measured as a function of the applied clear voltage. The I_{ds}-V_{cl} characteristics of the DEPFET Type-I is shown in Figure 3.9 (the blue curve). One can see that the JFET current remains almost unchanged as far as the clear voltage is lower than the reach-though voltage of the punch-through clear structure. Beyond this value, the internal gate potential varies in the same way as the clear potential and the JFET current decreases with the increasing clear voltage.

The JFET transconductance g_m determined from the current-voltage curve as $g_m = \partial I_{ds}/\partial V_{cl}$ is also plotted in Figure 3.9 (the red curve). The values of the transconductance are similar to ones obtained when the JFET is measured with the detector substrate undepleted (compare with Figure 3.2).

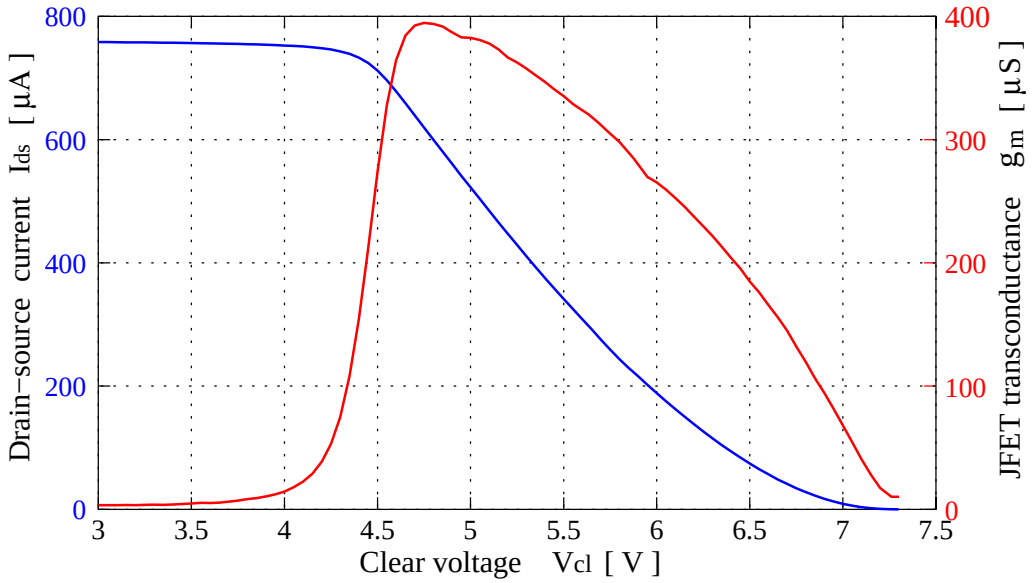


Figure 3.9: I_{ds}-V_{cl} characteristics of the DEPFET Type-I.

The same characteristics measured for the DEPFET Type-III (same clear structure, but different JFET) are plotted in Figure 3.10. The curves are similar to the ones

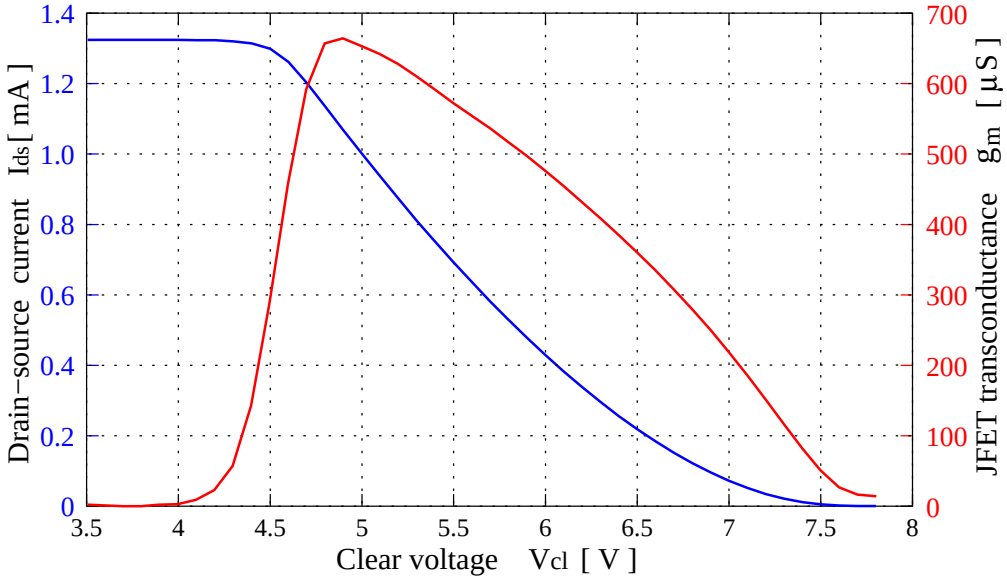


Figure 3.10: I_{ds}-V_{cl} characteristics of the DEPFET Type-III.

measured for the DEPFET Type-I, except that the JFET maximum current has larger values. Consequently, the JFET transconductance parameter is also larger.

Figure 3.11 shows the I_{ds}-V_{cl} characteristics of the DEPFET Type-II (same JFET as DEPFET Type-I, but with MOSFET clear structure). It can be seen that the JFET

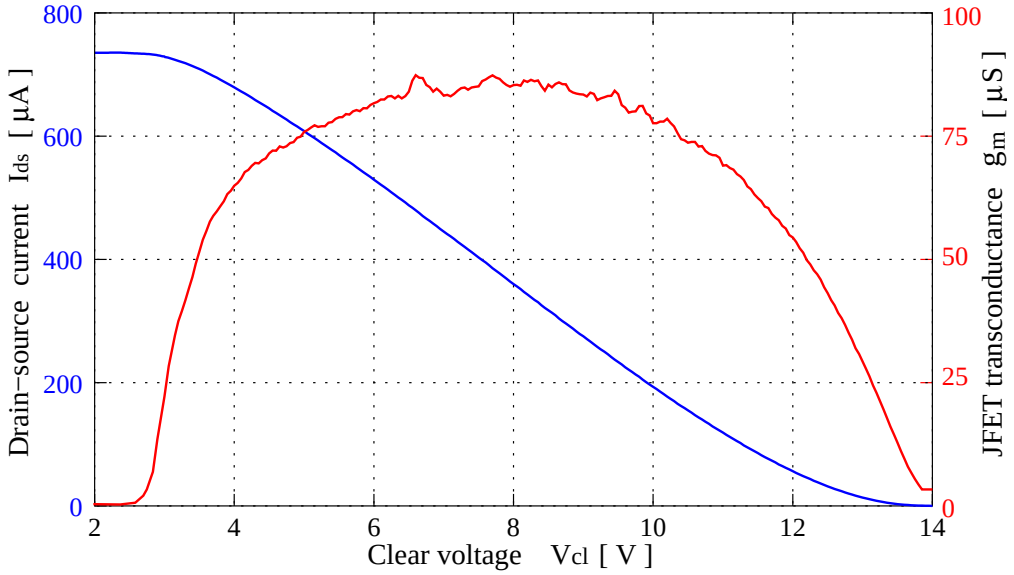


Figure 3.11: I_{ds}-V_{cl} characteristics of the DEPFET Type-II.

current decreases with the clear voltage for values larger than the threshold voltage of the MOSFET clear structure. In comparison to the previous DEPFET type, the voltage value at which the channel is pinched off (i.e. JFET current is zero) is much larger. Consequently, the JFET transconductance (the red curve) has lower values at similar current values.

The same characteristics measured for the last DEPFET type are shown in Figure 3.12. They show similarities with the DEPFET Type-II (also with MOSFET clear structure).

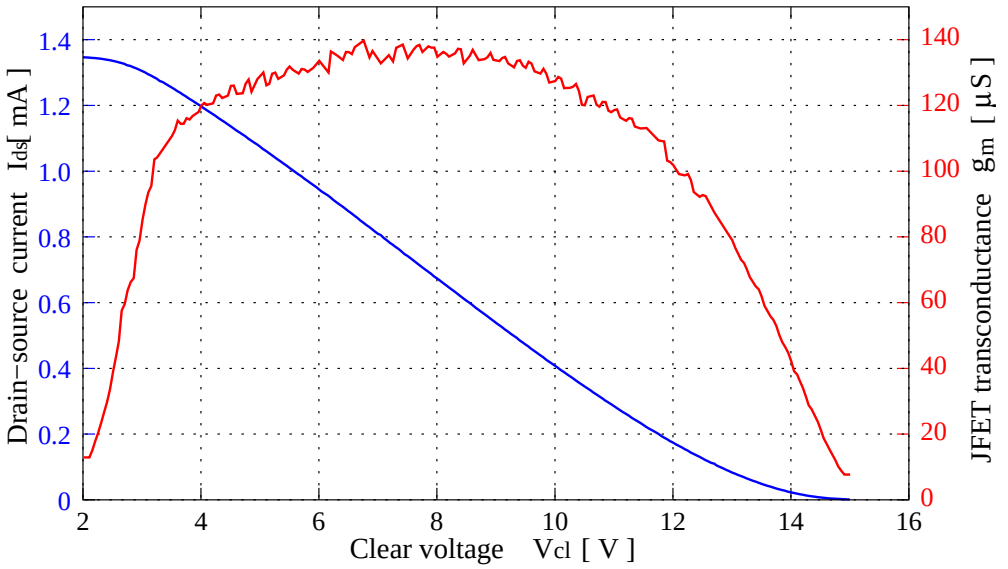


Figure 3.12: I_{ds}-V_{cl} characteristics of the DEPFET Type-IV.

Chapter 4

Small-signal and noise analysis of the DEPFET

The analytical analysis of the small-signal equivalent circuit of the continuous clear DEPFET device is performed in this chapter. The noise behavior of the device is also treated here.

4.1 Small-signal equivalent circuit of a JFET

Since the central element of the DEPFET detector is the JFET transistor, the small-signal equivalent circuit model of a JFET is briefly described in this section. The small-signal signal equivalent circuit model is used to described the behavior of any active device (e.g. JFET or MOSFET), when the device is biased to operate at a certain point on its static characteristic and a small AC signal is superimposed on the DC bias values.

Figure 4.1 shows a simplified model [Gray84] of the small-signal equivalent circuit of a JFET transistor in saturation. Since the gate-channel junction of the JFET is reverse

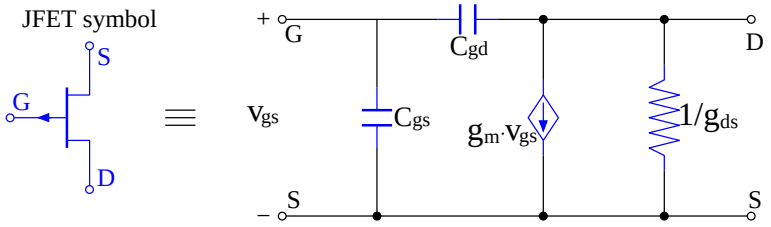


Figure 4.1: Small-signal equivalent circuit of a p-channel JFET.

biased, the gate is connected to source and drain only through the equivalent capacitances C_{gs} and C_{gd} of the gate-source and gate-drain depletion regions. The JFET channel is represented in the model by a voltage-controlled current source with the current flowing from drain to source. The current value is given by $i_{ds} = g_m v_{gs}$, where v_{gs} is the small AC voltage applied between gate and source and g_m is the JFET transconductance. The

output impedance $r_o = 1/g_{ds}$ (see equation 2.16) appears also in parallel to the current source.

4.2 Small-signal analysis of the DEPFET device

One can imagine two principial methods to read out the signal from a DEPFET device. In one of them, the drain-source voltage is kept at a constant value. The charge signal arriving at the internal gate produces a change in the drain-source current which can be further amplified by a current-voltage converter.

In the other method, only the drain node is kept to a fixed potential and a constant current (provided by a current source) flows into the JFET channel at the source. The signal charge in the internal gate causes a potential change at the gate. Since the drain-source current is constant, a similar voltage change takes place at the JFET source. This voltage change is then amplified and processed by appropriate electronics. Operated in this scheme, the JFET is said to be in a *source-follower* configuration (the source "follows" any voltage change at the gate).

The source-follower configuration has several advantages over the configuration with fixed drain-source voltage (also called *grounded-source* configuration). The signal rise time is smaller (i.e. readout can be faster), variations in the pinch-off voltage of the JFET transistor (operating within a DEPFET matrix) have no influence on the signal amplitude; the DEPFET can be DC decoupled from the subsequent electronics.

4.2.1 Source-follower configuration of the DEPFET

Figure 4.2a shows the electrical circuit in which the DEPFET is in the source-follower configuration. The DEPFET symbol is derived from that of a *p*-channel JFET transistor;

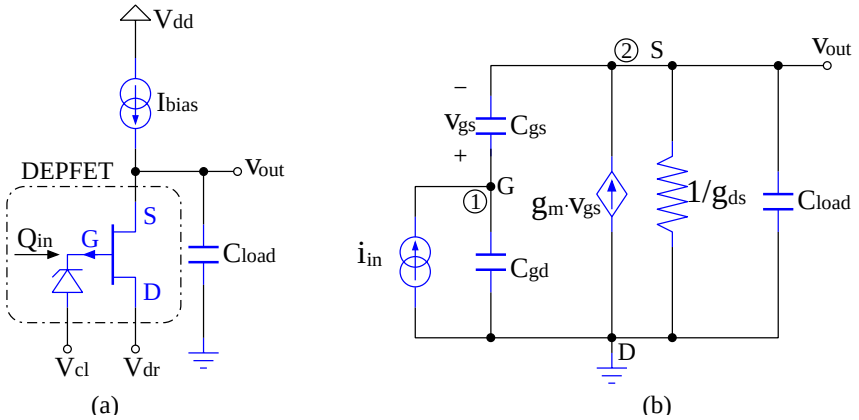


Figure 4.2: Small-signal equivalent circuit of a *p*-channel JFET.

the clear mechanism is represented by a diode due to the analogy of the clear characteristic to that of a forward biased diode. The JFET channel current is provided by a constant current source I_{bias}. A load capacitance C_{load} is added at the output node to account for

the parasitic capacitances of the output node and the input capacitance of the subsequent readout stage.

The equivalent small-signal circuit is drawn in Figure 4.2b. The input quantity - the signal charge Q_{in} - is represented by a current source with variable current $i_{in}(t) = dQ_{in}/dt$. Since the small-signal analysis is performed in the s-domain (Laplace transform of the time domain), $i_{in}(s) = sQ_{in}(s)$.

The voltage-charge transfer characteristic of the circuit is determined by applying Kirchoff's theorem for currents in the circuit nodes 1 and 2:

$$\begin{aligned} &\text{Node 1:} \quad -i_{in} + v_g sC_{gd} + (v_g - v_s)sC_{gs} = 0 \\ &\text{Node 2:} \quad g_m(v_g - v_s) - v_s(g_{ds} + sC_{load}) + (v_g - v_s)sC_{gs} = 0 \end{aligned} \tag{4.1}$$

Eliminating v_g from both equations and noting that $v_s = v_{out}$ and $i_{in} = sQ_{in}$, one obtains the voltage-charge transfer function:

$$A_{v-q}(s) = \frac{v_{out}}{Q_{in}} = \frac{1}{C_{gd}} \cdot \frac{1}{1 + \frac{g_{ds}}{g_m}\left(1 + \frac{C_{gs}}{C_{gd}}\right)} \cdot \frac{1 + \frac{s}{z_o}}{1 + \frac{s}{p_o}} \tag{4.2}$$

z_o and p_o are called *zero* and the *pole* [Sed98] of the transfer function and have the expressions:

$$\begin{aligned} z_o &= \frac{g_m}{C_{gs}} \\ p_o &= \frac{g_{ds} + g_m \frac{C_{gd}}{C_{gs}+C_{gd}}}{C_{load} + \frac{C_{gd}C_{gs}}{C_{gd}+C_{gs}}} \end{aligned} \tag{4.3}$$

The transfer function A_{v-q} can be re-written as:

$$A_{v-q}(s) = G \cdot \frac{1 + \frac{s}{z_o}}{1 + \frac{s}{p_o}} \tag{4.4}$$

where G is the low-frequency gain given by:

$$G = A_{v-q}(0) = \frac{1}{C_{gd}} \cdot \frac{1}{1 + \frac{g_{ds}}{g_m}\left(1 + \frac{C_{gs}}{C_{gd}}\right)} \tag{4.5}$$

Since $g_{ds} \ll g_m$ for a JFET in saturation, the gain factor can be approximated as:

$$G \approx \frac{1}{C_{gd}} \tag{4.6}$$

The above equation tells us that the gate-drain capacitance must be minimized in order to have large gain. Assuming a capacitance value of $C_{gd} = 10fF$, the gain factor is $G \approx 10^{14}V/C = 16\mu V/e^-$.

To study the effect of p_o and z_o in the transfer function, consider a numerical example for the DEPFET parameters:

$$\begin{aligned} C_{gs} &= 100\text{fF} \\ C_{gd} &= 10\text{fF} \\ g_m &= 100\mu S \\ g_{ds} &= 1\mu S \end{aligned}$$

The values of z_o and p_o are then:

$$\begin{aligned} z_o &= \frac{g_m}{C_{gs}} = 1GHz \\ p_o &= \frac{g_{ds} + g_m \frac{C_{gd}}{C_{gs}+C_{gd}}}{C_{load} + \frac{C_{gd}C_{gs}}{C_{gd}+C_{gs}}} \approx \frac{g_m}{C_{gs} + C_{load}\frac{C_{gs}+C_{gd}}{C_{gd}}} \approx z_o \frac{1}{1 + \frac{C_{load}}{C_{gd}}} \end{aligned} \tag{4.7}$$

The value of p_o is dependent on the load capacitance C_{load}. It is smaller than the value of z_o and approaches z_o for $C_{load} \to 0$. Replacing $s = j\omega = j2\pi f$ in the expression of $A_{v-q}(s)$, the normalized magnitude of A_{v-q} is plotted as a function of frequency in Figure 4.3 for different values of C_{load}. One can see that p_o determines the bandwidth

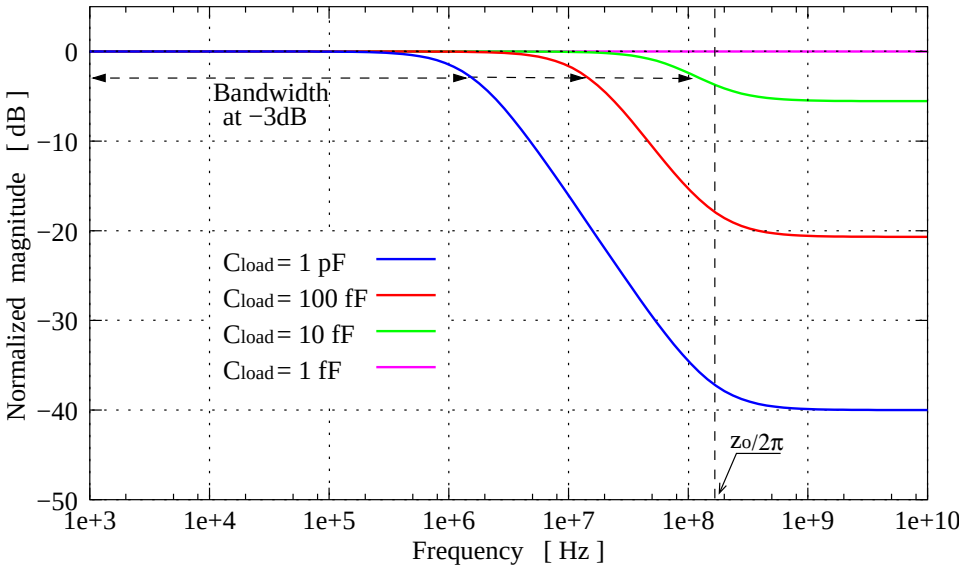


Figure 4.3: Normalized amplitude of the DEPFET transfer function.

of the transfer function and therefore, the rise time of the output signal. The DEPFET bandwidth decreases with increasing load capacitance.

The relation between p_o and the signal rise time t_r (calculated between 10% and 90% from the signal amplitude) is [Gray84]:

$$t_r = \frac{ln9}{p_o} \approx 2.2 \times \frac{C_{load} + \frac{C_{gd}C_{gs}}{C_{gd}+C_{gs}}}{g_{ds} + g_m \frac{C_{gd}}{C_{gs}+C_{gd}}} \tag{4.8}$$

Figure 4.4 shows the signal rise time plotted as a function of the load capacitance for two values of g_m. Typical values for C_{load} are in the range of few pF which correspond to

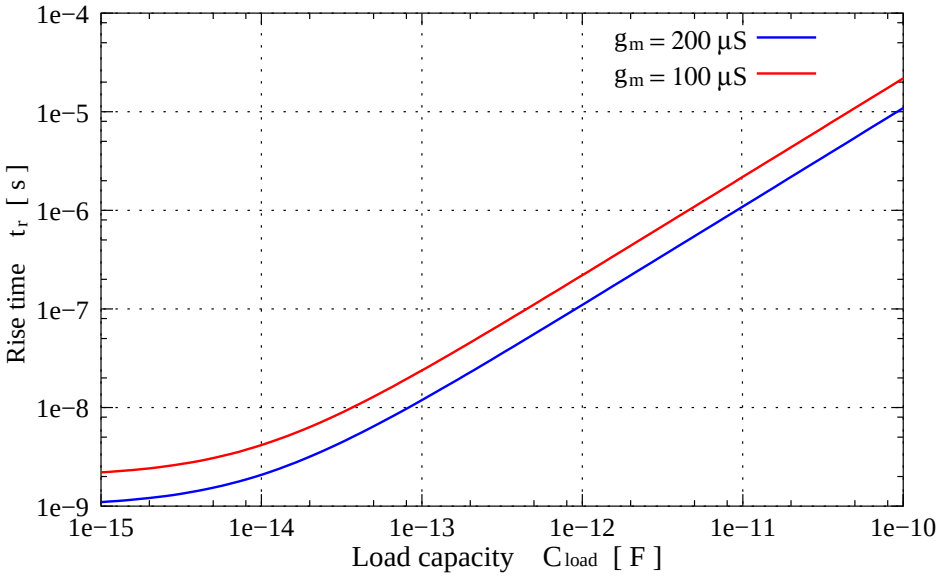


Figure 4.4: Signal rise time versus load capacitance.

rise time values of hundreds of *ns*.

Another parameter of interest which can be calculated from the small-signal analysis is the output impedance Z_o. The circuit for calculating Z_o is shown in Figure 4.5. With

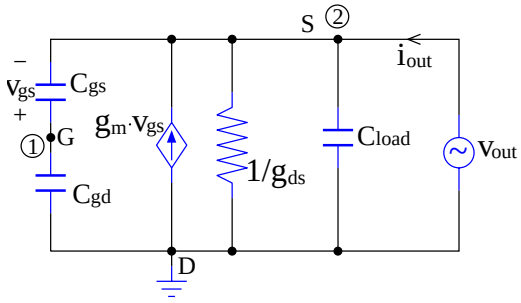


Figure 4.5: Small-signal circuit for calculating the output impedance.

no input signal applied ($i_{in} = 0$), a voltage source v_{out} is connected to the output node and the current i_{out} is calculated. The output impedance Z_o is give by :

$$Z_o = \frac{v_{out}}{i_{out}} \tag{4.9}$$

By applying the Kirchoff's theorem in the node 2:

$$i_{out} = v_{out} s C_{load} + v_{out} g_{ds} - g_m(v_g - v_s) - (v_g - v_s) s C_{gs} \tag{4.10}$$

The voltage v_g at the node 1 is given by:

$$v_g = v_s \frac{C_{gs}}{C_{gd} + C_{gs}} \quad \Rightarrow \quad v_g - v_s = -v_s \frac{C_{gd}}{C_{gs} + C_{gd}} = -v_{out} \frac{C_{gd}}{C_{gs} + C_{gd}} \tag{4.11}$$

Combining both equations, one obtains:

$$Z_o = \frac{v_{out}}{i_{out}} = \frac{R_o}{1 + \frac{s}{p_o}} \qquad with \qquad R_o = \frac{1}{g_{ds} + g_m \frac{C_{gd}}{C_{gs}+C_{gd}}} \tag{4.12}$$

p_o is the same pole that occurs in the expression of the transfer function A_{v-q}. Having determined the output impedance, the DEPFET circuit can be replaced with an equivalent circuit consisting of a controlled voltage source with the voltage value $A_{v-q} \cdot Q_{in}$ in series with the output impedance Z_o.

4.3 Noise analysis of the DEPFET

The term "noise" refers to small fluctuations in the voltage across, or in the current passing through an electronic device. The existence of noise is basically due to the fact that the electrical charge (involved in the transport processes) is not continuous, but is carried in discrete amounts (electrons and/or holes). The noise is thus associated with microscopic fluctuations in the movement of the charge carriers. To study the noise is important because it sets a lower limit to the quantities to be measured or to the signal to be amplified in an electronic device.

4.3.1 Noise sources in electronic devices

Shot noise
Shot noise is always associated with a current flow through a device and is a direct consequence of the discrete nature of the electrical charge. Consider for example the case of a diode with a constant current I flowing through it. The current consists of charge carriers (electrons and holes) passing from one side to the other side of the diode junction. The passage of each carrier across the junction is a purely random process. Thus the current I, which is supposed to be a steady current, is in fact composed of a large number of independent, random current pulses and the current fluctuates in time. The spectral power density of the shot noise current fluctuations is given by [Lak94]:

$$\frac{d\overline{i_{nI}^2}}{df} = 2q \cdot I \tag{4.13}$$

where q is the electron charge.

Thermal noise
Thermal noise is generated by the thermal motion of the electrons in a conductor or semiconductor material. It is unaffected by the presence or the absence of a voltage across the material, since the thermal velocities of the charge carriers are much higher than the drift velocities in the presence of an electrical field. The noise is proportional to the quantity responsible for the thermal motion which is the absolute temperature T. Considering the case of a resistor R, the spectral density of the thermal noise voltage is given by [Gray84]:

$$\frac{d\overline{u_{n,th}^2}}{df} = 4kTR \tag{4.14}$$

where k is the Boltzmann constant.

Flicker noise
The flicker noise (also called "1/f" noise or low-frequency noise) is present in all active devices. The physical source of this noise is not unique, but in the FET transistors it is caused mainly by the trapping centers (crystal defects) present in the transistor channel. While the shot noise and the thermal noise spectra are independent on frequency (so-called *white noise* sources), the spectral density of the flicker noise is frequency dependent and is given by [Gray84]:

$$\frac{d\overline{u^2_{n,1/f}}}{df} = \frac{A_n}{f^\alpha}, \qquad \alpha \approx 1 \tag{4.15}$$

Noise sources in FET transistors
There are two sources of noise that occur in the FET transistors. Figure 4.6 shows the small-signal equivalent circuit of a FET transistor with the noise sources. Due to the

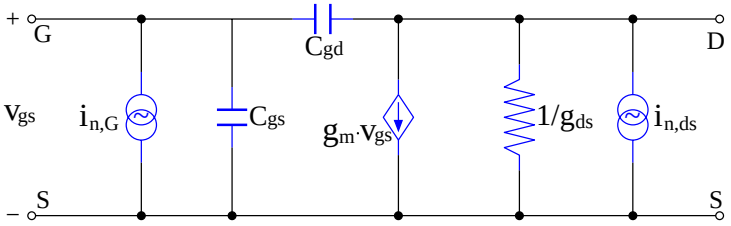


Figure 4.6: Small-signal circuit of a FET with noise sources.

small leakage current flowing into the transistor gate, a shot noise source represented by $i_{n,G}$ is present at the gate. Its spectral density is given by:

$$\frac{d\overline{i^2_{n,G}}}{df} = 2qI_G \tag{4.16}$$

where I_G is the gate leakage current.

The other noise source in a FET transistor appears as a current source in the transistor channel ($i_{n,ds}$ in Figure 4.6). It has two components: a thermal component due to the channel resistance and an "$1/f$" component due to the presence of trapping centers in the transistor channel. The spectral density of $i_{n,ds}$ is given by [Gray84]:

$$\frac{d\overline{i^2_{n,ds}}}{df} = \frac{d\overline{i^2_{n,th}}}{df} + \frac{d\overline{i^2_{n,1/f}}}{df} = \frac{8kT}{3}g_m + \frac{A_f}{f}g_m^2 \tag{4.17}$$

where A_f is a parameter which depends on the transistor dimensions and on material properties [Gray84, Lak94].

The shot noise plays a minor role in the JFET transistors (very small leakage current) and is completely absent in MOSFETs. "$1/f$" noise is very prominent in MOSFETs, but less significant in JFET transistors.

4.3.2 Statistical noise in semiconductor detectors

In the particle detection systems, apart from the electronic noise introduced by the readout circuit, one encounters an additional source of noise. This is related to the statistical process of particle energy loss by ionization and is referred as statistical noise. The origins of this noise in the semiconductor detectors are the statistical fluctuations in the process of generating electron-hole pairs by means of ionization [Lut99]. When an ionizing particle interacts with the semiconductor material, it creates electron-hole pairs that can be detected as electric signals. However, a fraction of the particle energy is converted into lattice vibrations (phonons). The energy of the phonons is a thermal energy and is not detected by the readout electronics. The number of generated charges has therefore statistical fluctuations. For a given energy of an incident particle, the number of electron-hole pairs generated in the detector fluctuates around a mean value given by [Lut99]:

$$N = \frac{E}{w} \tag{4.18}$$

where E is the total energy absorbed in the detector and w is the mean energy spent for creating a single electron-hole pair. For silicon, $w = 3.64eV$ at room temperature [Lec98]. The variance in the number of signal charges N is given by [Lut99]:

$$\overline{\Delta N^2} = F \cdot N = F\frac{E}{w} \tag{4.19}$$

where F is an dimensionless quantity and is called Fano factor; the statistical noise is also called Fano noise. The Fano factor depends very little on the energy. For silicon detectors [Per99], $F = 0.12 \div 0.15$ in the x-ray energy range.

4.3.3 Noise sources in the DEPFET device

For a more comprehensive treatment of the noise behaviour of the DEPFET device, consider the circuit drawn in Figure 4.7. The DEPFET is in the source-follower configuration and the output signal is further amplified by a feedback amplifier (operational core amplifier) and filtered by a filter with the transfer characteristic $H(s)$. The voltage amplification of the feedback amplifier is $-C_{in}/C_{fb}$. The noise sources are considered absent for the moment.

Performing a similar analysis to that in section 4.2.1, the voltage at the filter output is found to be:

$$v_{out}(s) = -\frac{i_{in}(s)}{s} \cdot G \cdot \frac{C_{in}}{C_{fb}} \cdot \frac{1+\frac{s}{z_o}}{1+\frac{s}{p_o}} H(s) \tag{4.20}$$

where G and z_o have the same values as in equations 4.5 and 4.3. The expression of p_o is identical to that in equation 4.3, except that C_{in} adds to the load capacitance C_{load} (C_{in} acts actually as a load capacitance for the DEPFET, since the node 3 in the above circuit is at virtual ground). The amplification factor of the feedback amplifier is C_{in}/C_{fb}.

Since the time needed by the signal electrons to drift to the internal gate is very short in comparison to the processing time of the readout, the time dependence of the input

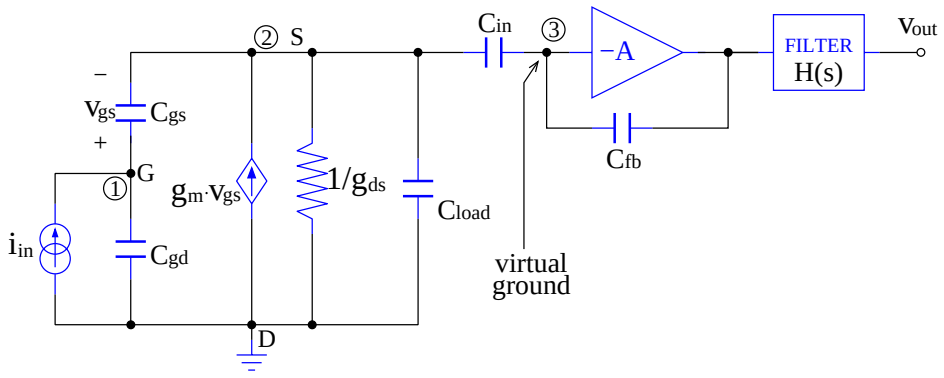


Figure 4.7: Small-signal circuit of the DEPFET with amplifier and filter.

charge $Q_{in}(t)$ can be approximated by a step function:

$$Q_{in}(t) = \begin{cases} 0 & \text{if } t < 0, \\ -Q_{sig} & \text{if } t \geq 0 \end{cases} \tag{4.21}$$

where $-Q_{sig}$ is the total charge at the internal gate. The input current is then $i_{in} = dQ_{in}(t)/dt = -Q_{sig}\delta(t)$. Since the Laplace transform of $\delta(t)$ is 1, $i_{in}(s) = -Q_{sig}$. Equation 4.20 becomes now:

$$v_{out,sig}(s) = Q_{sig} \cdot G \cdot \frac{C_{in}}{C_{fb}} \cdot \frac{1 + \frac{s}{z_o}}{1 + \frac{s}{p_o}} \cdot \frac{H(s)}{s} \tag{4.22}$$

The time dependence of the output signal is obtained by performing the inverse Laplace transform:

$$v_{out,sig}(t) = \mathcal{L}^{-1}\{v_{out,sig}(s)\} = Q_{sig} \cdot G \cdot \frac{C_{in}}{C_{fb}} \cdot \mathcal{L}^{-1}\left\{\frac{1 + \frac{s}{z_o}}{1 + \frac{s}{p_o}} \cdot \frac{H(s)}{s}\right\} \tag{4.23}$$

The maximum of this function is then used for further processing of the signal.

Consider now the different noise sources that occur in the circuit; the resulting circuit is shown in Figure 4.8. The DEPFET clear current (detector leakage current) gives rise to shot noise represented here by the current source $i_{n,cl}$ at the input. As pointed out in section 4.3.1, $i_{n,G}$ is the shot noise due to the gate leakage current and $i_{n,ds}$ is noise source of the JFET channel. The current source that biases the JFET introduces a current noise source $i_{n,bias}$ in parallel with the transistor channel noise $i_{n,ds}$. The noise contribution of the core amplifier employed in the feedback amplification is represented by its equivalent input noise sources $e_{n,a}$ (serial noise) and $i_{n,a}$ (parallel noise).

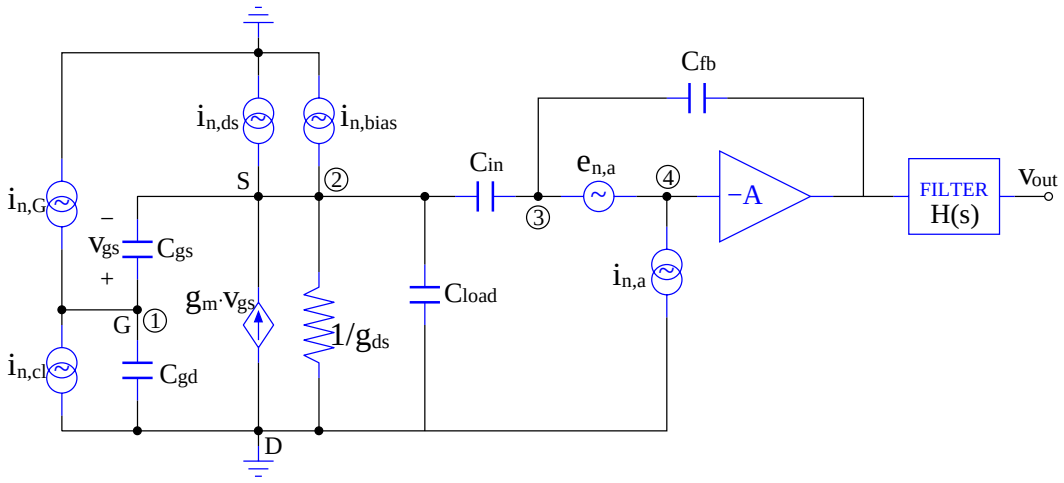


Figure 4.8: The noise sources in the small-signal circuit of the DEPFET.

It is a common practice in the particle detection systems to express the system noise in *equivalent noise charge* (ENC). This is the number of electron charges in the detector that produces an output signal equal to the total output noise of the system.

In the following treatment, all the noise sources are considered independent on each other, since they arise from separate noise mechanisms. Each noise source can thus be treated individually and its contribution is calculated separately. The mean-square value of the total noise contribution is calculated by adding the individual mean-square contributions from each source.

Noise contribution of $i_{n,cl}$

Comparing the circuits in Figure 4.8 and 4.7, it can be observed that $i_{n,cl}$ can be treated in the same way as the input current signal i_{in}. The corresponding output voltage is given therefore by equation 4.20:

$$v_{out,i_{n,cl}}(\omega) = -\frac{i_{n,cl}(j\omega)}{j\omega} \cdot G \cdot \frac{C_{in}}{C_{fb}} \cdot \frac{1+\frac{j\omega}{z_o}}{1+\frac{j\omega}{p_o}} H(j\omega) \tag{4.24}$$

where G, z_o and p_o are identical to those in equation 4.20 and $s = j\omega$. The root-mean-square value of the the output noise voltage is obtained by integrating over the whole frequency spectrum:

$$\begin{aligned} v^{rms}_{out,i_{n,cl}} &= \sqrt{\int_0^\infty v^2_{out,i_{n,cl}} df} = \sqrt{\frac{1}{2\pi}\int_0^\infty v^2_{out,i_{n,cl}}(\omega) d\omega} \\ &= \left[\frac{1}{2\pi}\int_0^\infty \frac{d\overline{i^2_{n,cl}}}{df} G^2 \left(\frac{C_{in}}{C_{fb}}\right)^2 \left|\frac{1+\frac{j\omega}{z_o}}{1+\frac{j\omega}{p_o}}\right|^2 \frac{|H(j\omega)|^2}{w^2} d\omega\right]^{\frac{1}{2}} \end{aligned} \tag{4.25}$$

The values of p_o and z_o are normally well beyond the filter bandwidth and their effect in

the above expression can be neglected. With $\frac{\overline{di^2_{n,cl}}}{df} = 2qI_{cl}$, equation 4.25 becomes:

$$v^{rms}_{out,i_{n,cl}} = \left[\frac{1}{2\pi}\cdot 2qI_{cl}\cdot G^2\left(\frac{C_{in}}{C_{fb}}\right)^2 \int_0^\infty \frac{|H(j\omega)|^2}{w^2}d\omega\right]^{\frac{1}{2}} \tag{4.26}$$

The equivalent input noise charge is determined by imposing:

$$\left(v^{rms}_{out,i_{n,cl}}\right)^2 = [max(v_{out,sig}(t))]^2 \tag{4.27}$$

where $v_{out,sig}(t)$ is the output voltage in response to the input charge Q_{sig}. Replacing $v^{rms}_{out,i_{n,cl}}$ and $v_{out,sig}(t)$ with their expressions from equations 4.26 and 4.23, one obtains:

$$Q^2_{i_{n,cl}} = q^2\cdot ENC^2_{i_{n,cl}} = 2qI_{cl}\frac{\frac{1}{2\pi}\int_0^\infty \frac{|H(j\omega)|^2}{w^2}d\omega}{max^2\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right)} \tag{4.28}$$

In calculating the integral $\int_0^\infty \frac{|H(j\omega)|^2}{w^2}$ it is useful to make the change of the variable $x = \omega\tau$, with τ being the time constant of the filter (also called shaping time). Equation 4.28 becomes:

$$ENC^2_{i_{n,cl}} = \frac{2I_{cl}}{q}\frac{\tau}{max^2\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right)}\frac{1}{2\pi}\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x^2}dx \tag{4.29}$$

or

$$\boxed{ENC^2_{i_{n,cl}} = \frac{2I_{cl}}{q}\tau A_1} \qquad A_1 = \frac{1}{2\pi}\frac{\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x^2}dx}{max^2\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right)} \tag{4.30}$$

The constant A is independent on the shaping time τ, but depends on the design of the filter.

Noise contribution of $i_{n,G}$
The gate leakage current has the same noise contribution as the clear current and the expression of *ENC* is given by:

$$\boxed{ENC^2_{i_{n,G}} = \frac{2I_G}{q}\tau A_1} \tag{4.31}$$

with A_1 from the equation 4.30.

Noise contribution of $i_{n,ds}$
Applying the Kirchoff's theorem for currents in the node 2 of the circuit, one obtains:

$$(v_g - v_s)sC_{gs} + g_m(v_g - v_s) - v_s g_{ds} - v_s(sC_{load} + sC_{in}) + i_{n,ds} = 0 \tag{4.32}$$

At the node 1 of the circuit:

$$v_g = v_s \frac{C_{gs}}{C_{gs}+C_{gd}} \quad \Rightarrow \quad v_g - v_s = -v_s \frac{C_{gd}}{C_{gs}+C_{gd}} \tag{4.33}$$

Combining the equations 4.32 and 4.33, one obtains:

$$v_s = \frac{i_{n,ds}}{g_m \frac{C_{gd}}{C_{gs}+C_{gd}} + g_{ds}} \cdot \frac{1}{1+\frac{s}{p_o}} \tag{4.34}$$

The output voltage is then:

$$v_{out,i_{n,ds}}(s) = -v_s \cdot \frac{C_{in}}{C_{fb}} \cdot H(s) = -\frac{i_{n,ds}}{g_m \frac{C_{gd}}{C_{gs}+C_{gd}} + g_{ds}} \cdot \frac{C_{in}}{C_{fb}} \cdot \frac{1}{1+\frac{s}{p_o}} H(s) \tag{4.35}$$

and its rms value is given by:

$$v_{out,i_{n,ds}}^{rms} = \left[\frac{1}{2\pi} \cdot \left(\frac{1}{g_m \frac{C_{gd}}{C_{gs}+C_{gd}} + g_{ds}} \right)^2 \left(\frac{C_{in}}{C_{fb}} \right)^2 \int_0^\infty \frac{\overline{di_{n,ds}^2}}{df} |H(j\omega)|^2 d\omega \right]^{\frac{1}{2}} \tag{4.36}$$

Recall that the JFET channel noise $i_{n,ds}$ has two components: the thermal noise and the flicker noise. The noise spectral density is given by:

$$\frac{\overline{di_{n,ds}^2}}{df} = \frac{8kT}{3} g_m + \frac{A_f}{f} g_m^2 \tag{4.37}$$

By applying the same procedure like in the case of $i_{n,cl}$, the equivalent noise charge contribution of the thermal noise component is found to be:

$$\boxed{ENC_{i_{n,th}}^2 = \frac{1}{q^2} \frac{8kT}{3g_m} (C_{gs}+C_{gd})^2 \frac{A_2}{\tau}} \qquad A_2 = \frac{1}{2\pi} \frac{\int_0^\infty |H(\frac{jx}{\tau})|^2 dx}{max^2 \left(\mathcal{L}^{-1} \left\{ \frac{H(s)}{s} \right\} \right)} \tag{4.38}$$

The contribution of the $1/f$ noise component is:

$$\boxed{ENC_{i_{n,1/f}}^2 = \frac{A_f}{q^2} (C_{gs}+C_{gd})^2 A_3} \qquad A_3 = \frac{\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x} dx}{max^2 \left(\mathcal{L}^{-1} \left\{ \frac{H(s)}{s} \right\} \right)} \tag{4.39}$$

Noise contribution of $i_{n,bias}$
Since $i_{n,bias}$ is in parallel with $i_{n,ds}$, the noise contribution of $i_{n,bias}$ is calculated in a similar way. The noise output voltage is given by equation 4.36, where $i_{n,ds}$ is replaced by $i_{n,bias}$. Supposing that the current source is a simple MOSFET transistor, its current noise density has also a thermal noise component and an "$1/f$" noise component:

$$\frac{\overline{di_{n,bias}^2}}{df} = \frac{8kT}{3} g_m^{bias} + \frac{B_f}{f} (g_m^{bias})^2 \tag{4.40}$$

where g_m^{bias} is the transconductance of the MOSFET transistor and B_f is the "$1/f$" noise coefficient of the MOSFET.

The values of the equivalent noise charge for each component are given by:

$$\boxed{ENC^2_{i_{n,bias^{th}}} = \frac{1}{q^2}\frac{8kT}{3}g_m^{bias}\left(\frac{C_{gs}+C_{gd}}{g_m}\right)^2\frac{A_2}{\tau}} \tag{4.41}$$

for the thermal component, and

$$\boxed{ENC^2_{i_{n,bias^{1/f}}} = \frac{B_f}{q^2}\left[\frac{g_m^{bias}}{g_m}(C_{gs}+C_{gd})\right]^2 A_3} \tag{4.42}$$

for the "$1/f$" component. A_2 and A_3 are the coefficients determined earlier.

Noise contribution of the amplifier

The equivalent circuit for determining the noise contribution of the amplifier is drawn in Figure 4.9 Since there is now input signal, the DEPFET circuit can be simply replaced

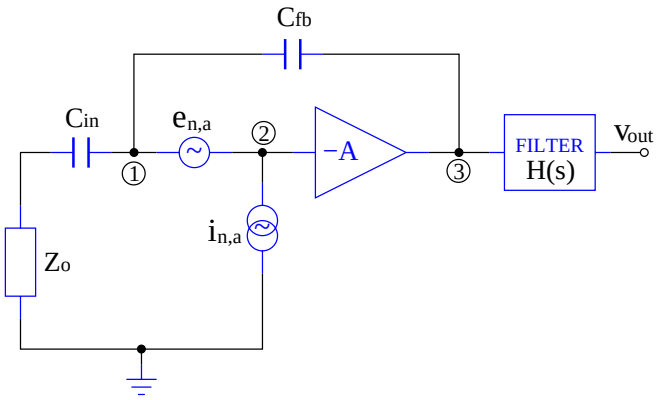


Figure 4.9: Equivalent circuit for determining the noise contribution of $e_{n,a}$ and $i_{n,a}$.

by the output impedance Z_o determined in equation 4.12.

Consider first the contribution of $i_{n,a}$ (set $e_{n,a} = 0$). The nodes 1 and 2 are at virtual ground and the current $i_{n,a}$ flows entirely through C_{fb}. At node 3 and output:

$$v_3 = \frac{i_{n,a}}{sC_{fb}} \qquad v_{out,i_{n,a}} = v_3 H(s) = \frac{i_{n,a}}{sC_{fb}}H(s) \tag{4.43}$$

The rms value of the output voltage is then:

$$v^{rms}_{out,i_{n,a}} = \left[\frac{1}{2\pi}\cdot\frac{1}{C^2_{fb}}\int_0^\infty \frac{d\overline{i^2_{n,a}}}{df}\frac{|H(j\omega)|^2}{\omega^2}d\omega\right]^{\frac{1}{2}} \tag{4.44}$$

and the equivalent noise charge contribution:

$$\boxed{ENC^2_{i_{n,a}} = \frac{1}{q^2}\frac{d\overline{i^2_{n,a}}}{df}\frac{1}{G^2}\frac{1}{C^2_{in}}A_1\tau} \tag{4.45}$$

To calculate the noise contribution of $e_{n,a}$ (set $i_{n,a} = 0$), one applies Kirchoff's theorem in node 1:

$$e_{n,a} = v_3 \frac{Z_o + \frac{1}{sC_{in}}}{Z_o + \frac{1}{sC_{in}} + \frac{1}{sC_{fb}}} \Rightarrow v_3 = e_{n,a}\left(1 + \frac{C_{in}}{C_{fb}} \cdot \frac{1}{1 + sC_{in}Z_o}\right) \tag{4.46}$$

The rms value of the output voltage is given by:

$$v_{out,e_{n,a}}^{rms} \approx \left[\frac{1}{2\pi} \cdot \left(1 + \frac{C_{in}}{C_{fb}}\right)^2 \int_0^\infty \frac{\overline{de_{n,a}^2}}{df} |H(j\omega)|^2 d\omega\right]^{\frac{1}{2}} \tag{4.47}$$

The amplifier serial noise $e_{n,a}$ is also composed of two terms: a white noise component $e_{n,a,th}$ (due to the thermal noise of the input FET), and a flicker noise component $e_{n,a,1/f}$. The expressions of the equivalent noise charge for each component are given by:

$$\boxed{ENC_{e_{n,a,th}}^2 = \frac{1}{q^2}\frac{\overline{de_{n,a,th}^2}}{df}\left(\frac{C_{in} + C_{fb}}{C_{in}}\right)^2 \frac{1}{G^2}\frac{A_2}{\tau}}$$
$$\boxed{ENC_{e_{n,a,1/f}}^2 = \frac{D_f}{q^2}\left(\frac{C_{in} + C_{fb}}{C_{in}}\right)^2 \frac{1}{G^2}A_3} \tag{4.48}$$

where G is the gain factor in equation 4.5 and D_f is the characteristic coefficient of the amplifier flicker noise.

All the noise sources discussed above and their contributions to the total value of the equivalent noise charge are summarized in Table 4.1.

Symbol	Description	Contribution in ENC^2
$i_{n,cl,G}$	Shot noise of the input leakage current	$\frac{2(I_{cl}+I_G)}{q}\tau A_1$
$i_{n,th}$	Thermal noise of the JFET channel	$\frac{1}{q^2}\frac{8kT}{3g_m}\left(C_{gs}+C_{gd}\right)^2\frac{A_2}{\tau}$
$i_{n,bias^{th}}$	Thermal noise of the bias MOSFET	$\frac{1}{q^2}\frac{8kT}{3}g_m^{bias}\left(\frac{C_{gs}+C_{gd}}{g_m}\right)^2\frac{A_2}{\tau}$
$i_{n,1/f}$	1/f noise from of the JFET channel	$\frac{A_f}{q^2}\left(C_{gs}+C_{gd}\right)^2 A_3$
$i_{n,bias^{1/f}}$	1/f noise of the bias MOSFET	$\frac{B_f}{q^2}\left[\frac{g_m^{bias}}{g_m}\left(C_{gs}+C_{gd}\right)\right]^2 A_3$
$e_{n,a,th}$	Serial input noise of the amplifier (thermal)	$\frac{1}{q^2}\frac{\overline{de_{n,a}^2}}{df}\left(\frac{C_{in}+C_{fb}}{C_{in}}\right)^2\frac{1}{G^2}\frac{A_2}{\tau}$
$e_{n,a,1/f}$	Serial input noise of the amplifier ("1/f")	$\frac{D_f}{q^2}\left(\frac{C_{in}+C_{fb}}{C_{in}}\right)^2\frac{1}{G^2}A_3$
$i_{n,a}$	Parallel input noise of the amplifier	$\frac{1}{q^2}\frac{\overline{di_{n,a}^2}}{df}\frac{1}{G^2}\frac{1}{C_{in}^2}A_1\tau$

Table 4.1: Noise sources in the DEPFET device

The total noise contribution is :

$$\boxed{\begin{aligned} ENC_{tot}^2 = ENC_{i_{n,cl,G}}^2 + ENC_{i_{n,th}}^2 + ENC_{i_{n,1/f}}^2 + ENC_{i_{n,bias^{th}}}^2 \\ + ENC_{i_{n,bias^{1/f}}}^2 + ENC_{e_{n,a,th}}^2 + ENC_{e_{n,a,1/f}}^2 + ENC_{i_{n,a}}^2 \end{aligned}}$$

It can be seen from Table 4.1 that all the parallel noise sources (shot noise of the leakage current, input current noise of the amplifier) have *ENC* contributions that are direct proportional to the shaping time. The contribution of the thermal noise sources (JFET, the bias MOSFET and the input FET of the amplifier) are inverse proportional to the shaping time. The flicker noise terms are independent on the shaping time. This shaping time dependence of ENC_{tot} results in an optimal shaping time at which ENC_{tot} has a minimum.

Numerical example
In order to plot ENC_{tot} as a function of the shaping time, consider the following numerical example:

- *DEPFET parameters*
  - $C_{gd} = 20fF$, $C_{gs} = 100fF$
  - $g_m = 100\mu S$, $g_{ds} = 2\mu S$
  - $I_{cl} + I_G = 8pA$
  - $A_f = 2 \times 10^{-13}V^2$
- *Bias transistor parameters*
  - $g_m^{bias} = 100\mu S$
  - $B_f = 5 \times 10^{-13}V^2$
- *Amplifier parameters*
  - $C_{in} = 500fF$, $C_{fb} = 25fF$
  - $\frac{\overline{de_{n,a,th}^2}}{df} = 4 \times 10^{-16}V^2/Hz$, $\frac{\overline{di_{n,a}^2}}{df} = 1 \times 10^{-28}A^2/Hz$
  - $D_f = 1 \times 10^{-11}V^2$
- *Filter parameters*
  - Semi-gaussian filter of the 1^{st} order: $H(s) = \frac{s\tau}{(1+s\tau)^2}$
  - $A_1 = A_2 = e^2/8$, $A_3 = e^2/2$ (see Appendix B)

Figure 4.10 shows the ENC contribution of each noise source, as well as the total ENC plotted as a function of the shaping time. One can see that the most relevant noise sources are the input shot noise (blue curve) due to the detector leakage current and the thermal noise of the JFET (green curve) and of the bias MOSFET transistor (red curve). ENC_{tot} (black curve) has a minimum of about $15e^-$ at a shaping time of $\tau \approx 1\mu s$.

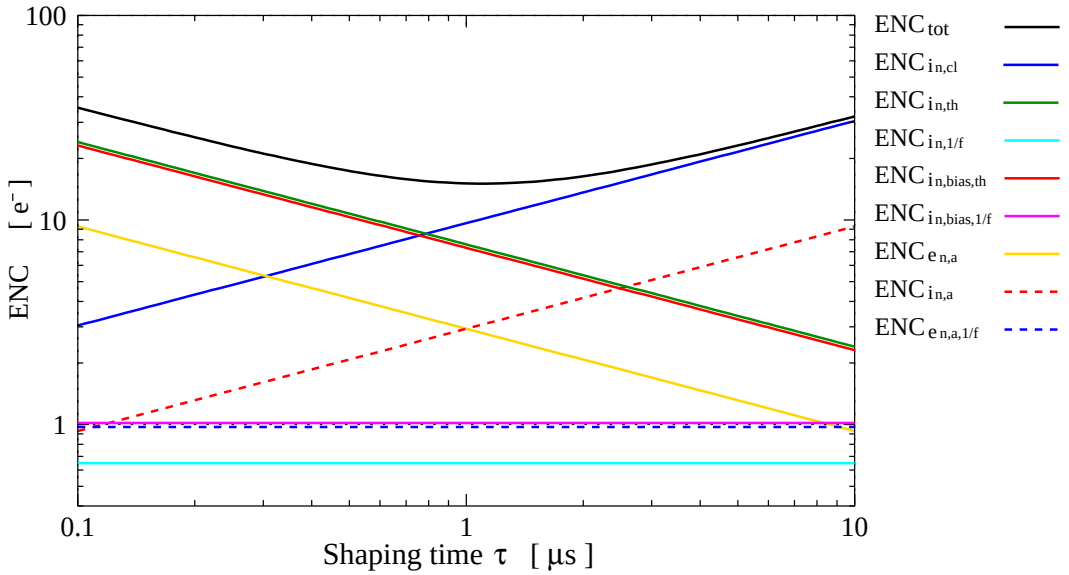


Figure 4.10: ENC as a function of the shaping time.

Chapter 5

Analog readout in CMOS technology

This chapter describes the analog readout for the continuous clear DEPFET detector. As we already discussed in the previous chapter, there are two possibilities to read out the signal from the DEPFET device: the source-follower configuration and the grounded-source configuration. In the source-follower configuration, the DEPFET responds with a voltage change to an input signal charge, while in the grounded-source configuration it responds with a current change. The subsequent amplifier stage should be a voltage amplifier for the source-follower configuration or a current amplifier for the grounded-source configuration. There are few advantages (pointed out in section 4.2) of the source-follower configuration over the grounded-source configuration. Therefore, we chose to design an analog readout for the DEPFET in the source-follower configuration. The readout is realized as a dedicated ASIC[1] in CMOS technology, with the choice of the AMS[2] 0.6 μm process. Figure 5.1 shows the the block diagram of the DEPFET readout. It consists of a bias current source for the JFET transistor integrated on the DEPFET

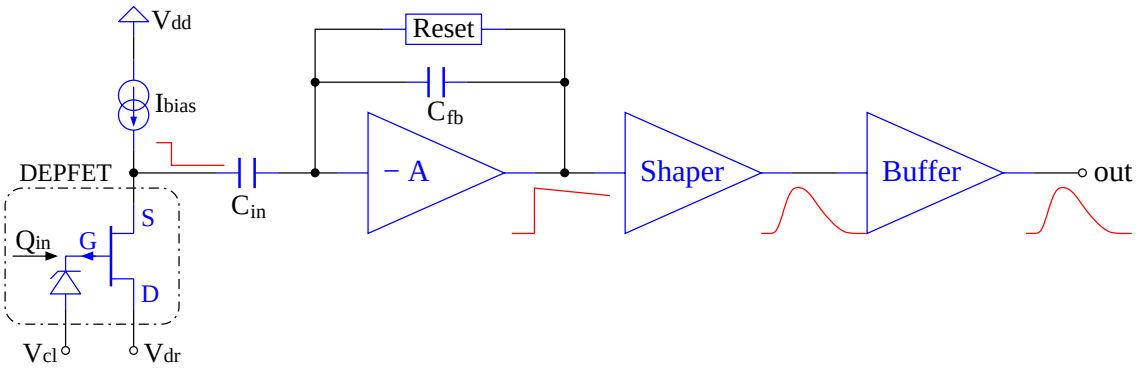


Figure 5.1: Block diagram of the DEPFET analog readout.

detector, a voltage feedback amplifier and a shaper to amplify and process the DEPFET output signal. The shaper output signal is buffered by an unity output buffer in order to be able to drive large capacitive loads (e.g. oscilloscope probe or coaxial cable capacitances).

[1] Application Specific Integrated Circuit
[2] Austria Micro Systems

Before continuing with a detailed description of each stage, a few remarks on the readout requirements should be pointed out. The main requirement that should be met is that the readout contributes with small noise to the total DEPFET noise. A detailed theoretical analysis regarding the noise is carried out in the next section.

Since the charge collected in the detector internal gate consists of electrons, it generates a negative voltage change at the DEPFET output. The amplifier should be designed for unipolar negative input voltage; this assigns the polarity of the input transistor (in the core amplifier) to an NMOS type. Regarding the frequency bandwidth of the amplifier, its upper limit must be higher than the upper limit of the DEPFET bandwidth (in Figure 4.3). With the DEPFET parameters given at the end of section 4.3, the 3-dB frequency limit is about 2 MHz, for $1pF$ load capacitance.

The DEPFET detector is not intended to be used at high rates of incident particles, thus the amplifier reset mechanism can be a slow reset. Following the noise calculation in the last chapter, the shaper should be designed with a shaping time in the μs range.

The analog readout is forseen to be implemented later on in readout matrix for a DEPFET matrix structure. The DEPFET matrix consists of hexagonal pixels, with the pitches of 140 μm on one axis and 120 μm on the complementary axis. Therefore, the design area of the analog readout should be less[3] than the pixel area.

5.1 Noise considerations

5.1.1 Noise optimization of the DEPFET bias current source

As shown in the last chapter, the DEPFET bias current source contributes to the DEPFET noise just as much as the JFET channel. It is therefore important to keep its noise contribution as low as possible. The basic current source configuration in CMOS technology is the so-called *current mirror* shown in Figure 5.2a. The central element of the circuit is the transistor T_1 whose gate is shorted to drain[4] and thus is operating in the saturation region. The drain-source current is given by [Alle02]:

$$I_{ds1} = I_{ref} = \frac{1}{2} k'_p \left(\frac{W}{L}\right)_1 (V_{gs1} - V_{tp})^2 \tag{5.1}$$

where k'_p is the transconductance parameter and V_{tp} is the threshold voltage of the PMOS transistor. The Early effect is neglected here ($\lambda = 0$). On the other hand:

$$I_{ref} = \frac{V_{dd} - V_{ref} - V_{gs1}}{R} \tag{5.2}$$

Combining both equations one obtains:

$$I_{ref} = \frac{2\Delta V}{\sqrt{\frac{2}{k'_p}\left(\frac{L}{W}\right)_1} + \sqrt{4\Delta V \cdot R + \frac{2}{k'_p}\left(\frac{L}{W}\right)_1}} \tag{5.3}$$

[3] In a matrix readout configuration there is also control logic circuitry present in each pixel

[4] The transistor is said to be diode-connected

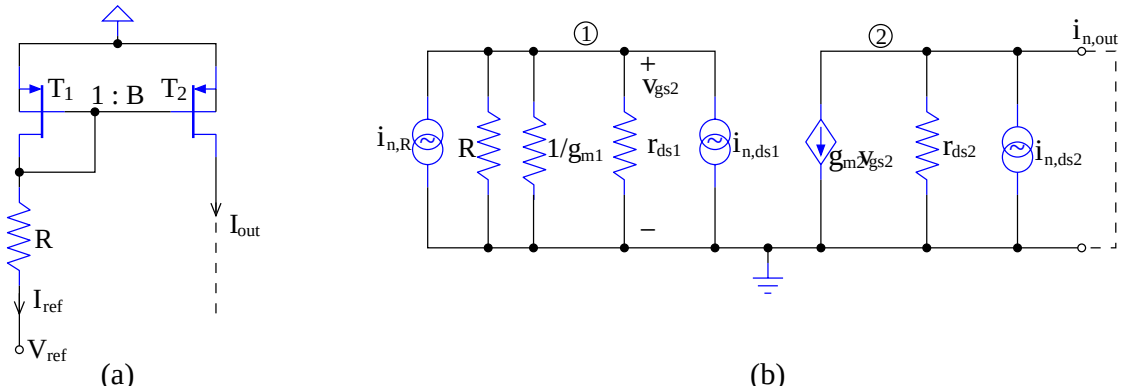


Figure 5.2: (a) PMOS current mirror; (b) Small-signal model with noise sources.

where $\Delta V = V_{dd} - V_{ref} - V_{tp}$.

The transistor T_2 has the same gate-source voltage as T_1. Assuming that T_2 is also operated in saturation, its drain-source current (the output current of the current source) is given by:

$$I_{ds2} = I_{out} = \frac{1}{2} k'_p \left(\frac{W}{L}\right)_2 (V_{gs2} - V_{tp})^2 \tag{5.4}$$

Since $V_{gs1} = V_{gs2}$, it follows that:

$$I_{out} = I_{ref} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} = I_{ref} B \tag{5.5}$$

where B is the ratio of the aspect ratios of the transistors T_2 and T_1 (B is called also current gain). The output current in transistor T_2 is given by the reference current in transistor T_1 multiplied by the current transfer ratio B.

Consider now the small-signal equivalent circuit model in Figure 5.2b, with all the noise sources that occur here: $i_{n,R}$ - the noise contribution of R, $i_{n,ds1}$ and $i_{n,ds2}$ - the noise contribution of T_1 and T_2, respectively. The total output noise current $i_{n,out}$ is found by shorting the output to ground and is given by:

$$i_{n,out} = -g_{m2} v_{gs2} + i_{n,ds2} \tag{5.6}$$

The voltage v_{gs2} between the node 1 and ground is given by:

$$v_{gs2} = -(i_{n,R} + i_{n,ds1}) \cdot (R \parallel (1/g_{m1}) \parallel r_{ds1}) \tag{5.7}$$

Assuming that that $1/g_{m1} \ll r_{ds1}$ and replacing v_{gs2} into equation 5.6, one obtains:

$$i_{n,out} \approx i_{n,ds2} + \frac{g_{m2}}{g_{m1}} \frac{R}{R + 1/g_{m1}} (i_{n,R} + i_{n,ds1}) = i_{n,ds2} + B'(i_{n,R} + i_{n,ds1}) \tag{5.8}$$

where $B' = B \frac{R}{R+1/g_{m1}} \leq B$. Since $i_{n,R}$, $i_{n,ds1}$ and $i_{n,ds2}$ are independent, the spectral power density of the output noise is:

$$\frac{d\overline{i^2_{n,out}}}{df} = \frac{d\overline{i^2_{n,ds2}}}{df} + B'^2 \left(\frac{d\overline{i^2_{n,R}}}{df} + \frac{d\overline{i^2_{n,out}}}{df} \right) \tag{5.9}$$

$i_{n,R}$ contains only the resistor thermal noise, $i_{n,ds1}$ and $i_{n,ds2}$ contain both thermal and flicker noise. Hence, the output noise can be separated into a thermal noise term and a flicker noise term:

$$\begin{aligned}
\frac{\overline{di^2_{n,out}}}{df} &= \frac{\overline{di^2_{n,out,th}}}{df} + \frac{\overline{di^2_{n,out,1/f}}}{df} \\
\frac{\overline{di^2_{n,out,th}}}{df} &= \frac{8kT}{3} g_{m2} + B'^2 \left(\frac{8kT}{3} g_{m1} + \frac{4kT}{R} \right) = \frac{8kT}{3} g_{m2,eq} \\
\frac{\overline{di^2_{n,out,1/f}}}{df} &= \frac{K_f}{(WL)_2 C^2_{ox}} g^2_{m2} + B'^2 \frac{K_f}{(WL)_1 C^2_{ox}} g^2_{m1} = \frac{K'_f}{(WL)_2 C^2_{ox}} g^2_{m2}
\end{aligned} \tag{5.10}$$

where K_f is the flicker noise coefficient [Lak94] of the PMOS transistor, C_{ox} is the capacity of the gate-oxide per unit area, W and L are the gate width and length. The parameters $g_{m2,eq}$ and K'_f are given by:

$$\begin{aligned}
g_{m2,eq} &= g_{m2} \left(1 + B \frac{R^2}{(R + 1/g_{m1})^2} \right) + \frac{3B^2 R}{2(R + 1/g_{m1})^2} \\
K'_f &= K_f \left(1 + B \frac{R^2}{(R + 1/g_{m1})^2} \frac{L^2_2}{L^2_1} \right)
\end{aligned} \tag{5.11}$$

Looking at the expressions 5.10 and 5.11, the total noise of the current source is minimized at first by choosing the transistors T_2 with small g_m and large gate area. The noise contribution of T_1 and R is further minimized by choosing the current gain B and the resistance R as low as possible. As a numerical example, for $B = 0.6$, $R = 1K\Omega$ and $g_{m2} = 50\mu S$, T_1 and R contribute only with 6% to the total thermal noise, while the flicker noise contribution of T_1 as practically null ($K'_f \approx K_f$).

5.1.2 Noise optimization of the feedback amplifier

The total noise contribution of the analog readout is determined by the amplifier. Hence, a close attention must be payed to the optimization of the amplifier noise. The circuit for studying the amplifier noise behavior is shown in Figure 5.3. The DEPFET is represented by its output impedance Z_o. In addition to the circuit in Figure 4.9, the input capacitance C_{ia} of the amplifier input transistor is also considered here. It will be seen later that C_{ia} plays an important role in the noise optimization procedure.

In a reasonable design, the total noise performance of the amplifier is governed by the noise performance of the input transistor. The equivalent input noise voltage of the amplifier $e_{n,a}$ can be therefore considered as the equivalent noise voltage of the input transistor. Its spectral density is given by [Lak94]:

$$\frac{\overline{de^2_{n,a}}}{df} = \frac{8kT}{3g_{m1}} + \frac{K_f}{W \cdot L \cdot C^2_{ox}} \frac{1}{f} \tag{5.12}$$

where g_{m1} is the transconductance of the input transistor, W and L are the gate width and length and C_{ox} is the gate-oxide capacitance per unit area. K_f is the flicker noise

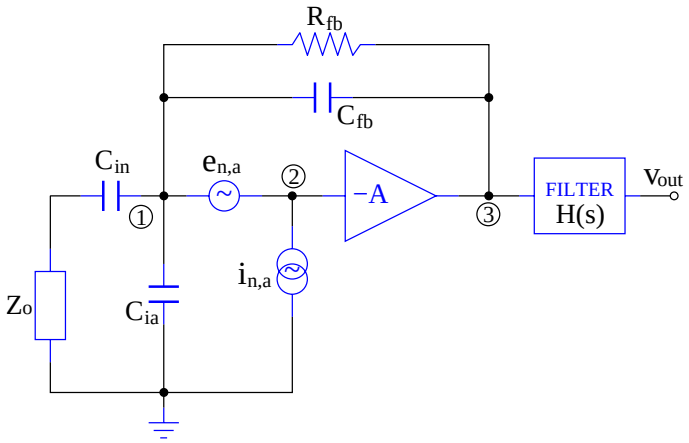


Figure 5.3: Equivalent circuit for studying the amplifier noise contribution.

coefficient. The first term in equation 5.12 represents the channel thermal noise, while the second term represents the flicker noise. Similar to the procedure applied in section 4.3, the noise contribution of the $e_{n,a}$ to the total noise is given by:

$$\begin{aligned} ENC^2_{e_{n,a}} &= ENC^2_{e_{n,a,th}} + ENC^2_{e_{n,a,1/f}} \\ ENC^2_{e_{n,a,th}} &= \frac{1}{q^2}\left(\frac{C_{in}+C_{fb}+C_{ia}}{C_{in}}\right)^2 \frac{8kT}{3g_{m1}} \cdot \frac{1}{G^2}\frac{A_2}{\tau} \\ ENC^2_{e_{n,a,1/f}} &= \frac{1}{q^2}\left(\frac{C_{in}+C_{fb}+C_{ia}}{C_{in}}\right)^2 \frac{K_f}{W \cdot L \cdot C^2_{ox}} \cdot \frac{1}{G^2} A_3 \end{aligned} \tag{5.13}$$

Apart from the constant factors G, A_2, A_3 (determined in section 4.3) and the filter time constant τ, the expressions 5.13 depend on the parameters of the input transistor and on the capacitances in the feedback network.

The input capacitance of the amplifier is given by [Cha97]:

$$C_{ia} = C_{gs1} + C_{gd1} = \frac{2}{3}WLC_{ox} + 2WL_DC_{ox} = \frac{2}{3}W\alpha LC_{ox} \tag{5.14}$$

where $\alpha L = L + 3L_D$ with L_D being the diffusion length of the source and drain implants under the transistor gate. Replacing C_{in} with the above expression and g_{m1} with $\sqrt{2k'I_{ds1}}\sqrt{W/L}$, the equations 5.13 become:

$$\begin{aligned} ENC^2_{e_{n,a,th}} &= \frac{1}{q^2}\left(\frac{C_{in}+C_{fb}+\frac{2}{3}W\alpha LC_{ox}}{C_{in}}\right)^2 \frac{8kT}{3\sqrt{2k'I_{ds1}}\sqrt{W/L}} \cdot \frac{1}{G^2}\frac{A_2}{\tau} \\ ENC^2_{e_{n,a,1/f}} &= \frac{1}{q^2}\left(\frac{C_{in}+C_{fb}+\frac{2}{3}W\alpha LC_{ox}}{C_{in}}\right)^2 \frac{K_f}{W \cdot L \cdot C^2_{ox}} \cdot \frac{1}{G^2} A_3 \end{aligned} \tag{5.15}$$

Minimization of $ENC_{e_{n,a,th}}$

Considering the dependence of $ENC_{e_{n,a,th}}$ on the parameter W, it can be derived that

an optimal input transistor gate width W_{opt} exists at which $ENC_{e_{n,a,th}}$ is minimum. The value of W_{opt} is found by solving for:

$$\frac{\partial ENC_{e_{n,a,th}}}{\partial W} = 0 \tag{5.16}$$

and is given by:

$$W_{opt} = \frac{C_{in} + C_{fb}}{2C_{ox}\alpha L} \tag{5.17}$$

The value of $ENC_{e_{n,a,th}}$ at the optimal gate width is given by:

$$ENC^{min}_{e_{n,a,th}} = \frac{4}{3qG}\frac{C_{in} + C_{fb}}{C_{in}}\sqrt{\frac{8kT}{3}\frac{\sqrt{\alpha}L}{\sqrt{\mu I_{ds1}(C_{in} + C_{fb})}}\frac{A_2}{\tau}} \tag{5.18}$$

where μ is the carrier mobility in the input transistor channel. Assuming a fixed gain $G_{fb} = C_{in}/C_{fb}$ of the feedback amplifier, equation 5.18 becomes:

$$ENC^{min}_{e_{n,a,th}} = \frac{4}{3qG}\left(1 + \frac{1}{G_{fb}}\right)\sqrt{\frac{8kT}{3}\frac{\sqrt{\alpha}L}{\sqrt{\mu I_{ds1}(1 + G_{fb})C_{fb}}}\frac{A_2}{\tau}} \tag{5.19}$$

The thermal noise contribution of the input transistor is minimized by choosing the minimum gate length (the technological limit), the maximum bias current I_{ds} (allowed by the power budget), maximum gain factor G_{fb} and large feedback capacitance C_{fb}. $ENC_{e_{n,a,th}}$ is plotted in Figure 5.4 as a function of the transistor gate width W for different values of C_{fb}.

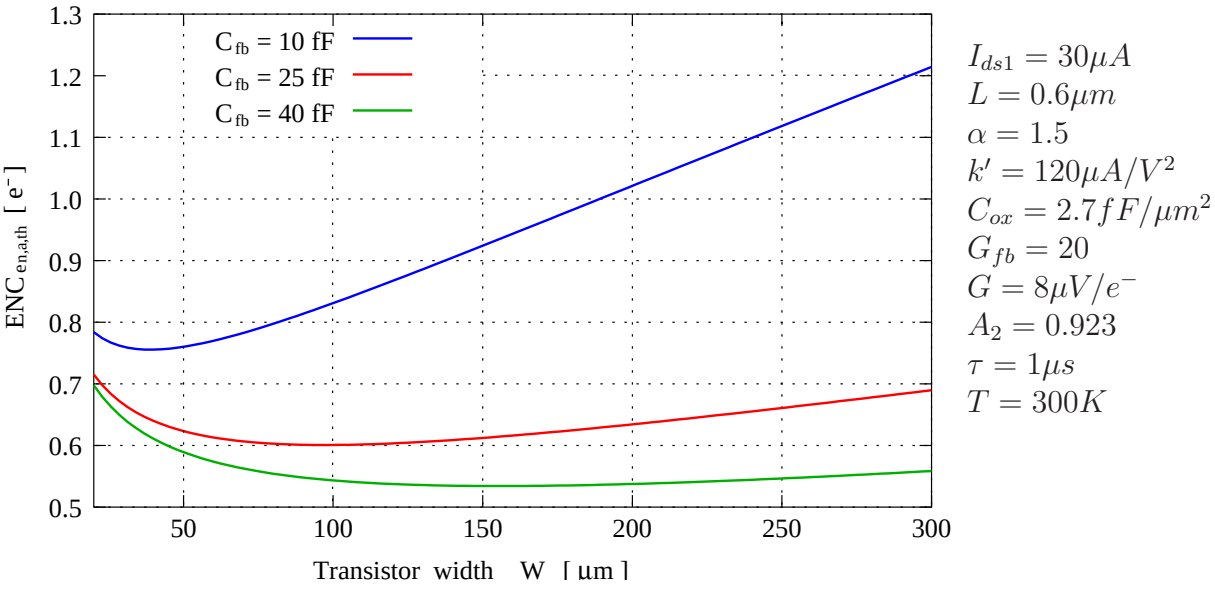


Figure 5.4: Thermal noise contribution of the input transistor.

The equivalent noise charge has a minimum at the optimal gate width and depends strongly on the feedback capacitance C_{fb}.

Minimization of $ENC_{e_{n,a,1/f}}$
Looking at the expression of $ENC_{e_{n,a,1/f}}$ in equation 5.15, it can be observed that the flicker noise contribution is minimum for an optimal value of the input transistor gate area which is found by solving:

$$\frac{\partial ENC_{e_{n,a,1/f}}}{\partial(WL)} = 0 \tag{5.20}$$

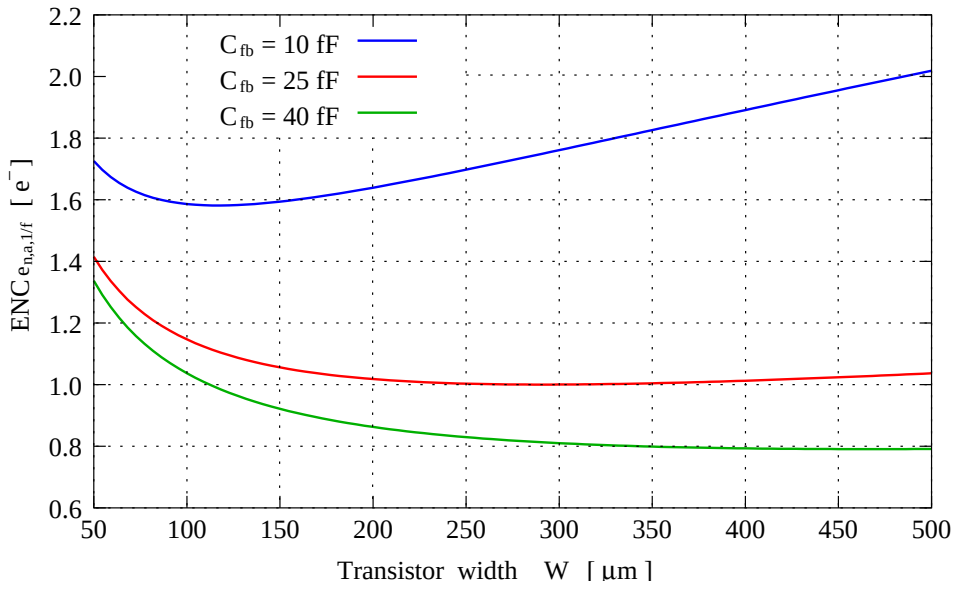
The optimal gate area is given by:

$$(WL)_{opt} = \frac{3(C_{in} + C_{fb})}{2\alpha C_{ox}} \tag{5.21}$$

and the minimum value of the flicker noise contribution is:

$$ENC^{min}_{e_{n,a,1/f}} = \frac{1}{qG}\left(1 + \frac{1}{G_{fb}}\right)\sqrt{\frac{8\alpha K_f A_3}{3C_{ox}(1+G_{fb})C_{fb}}} \tag{5.22}$$

Figure 5.5 shows the dependence of $ENC_{e_{n,a,1/f}}$ on the gate width for the same values of C_{fb} as in the previous case.



$L = 0.6\mu m$
$\alpha = 1.5$
$C_{ox} = 2.7fF/\mu m^2$
$K_f = 4{\cdot}10^{-27}C^2/m^2$
$G_{fb} = 20$
$G = 8\mu V/e^-$
$A_3 = 3.69$

Figure 5.5: Flicker noise contribution of the input transistor.

Minimization of the total amplifier noise
The total noise contribution of the amplifier is obtained by adding the noise contributions of $e_{n,a}$ (determined above) and $i_{n,a}$. The equivalent input noise current $i_{n,a}$ is basically the thermal noise current of the feedback resistance R_{fb}. Its spectral density is given by:

$$\frac{d\overline{i^2_{n,a}}}{df} = \frac{4kT}{R_{fb}} \tag{5.23}$$

The ENC contribution of $i_{n,a}$ is given by equation 4.45:

$$ENC_{i_{n,a}} = \frac{1}{qG}\frac{1}{C_{in}}\sqrt{\frac{4kT}{R_{fb}}A_1\tau} = \frac{1}{qG}\frac{1}{G_{fb}C_{fb}}\sqrt{\frac{4kT}{R_{fb}}A_1\tau} \tag{5.24}$$

$ENC_{i_{n,a}}$ is minimized by choosing a large feedback resistance, large feedback capacitance and large feedback gain. The total noise contribution of the amplifier is:

$$ENC_{a,tot} = \sqrt{ENC^2_{e_{n,a,th}} + ENC^2_{e_{n,a,1/f}} + ENC^2_{i_{n,a}}} \tag{5.25}$$

and is plotted in Figure 5.6 as a function of the input transistor gate width, for different values of C_{fb}. The feedback resistance value is assumed to be as high as $1G\Omega$.

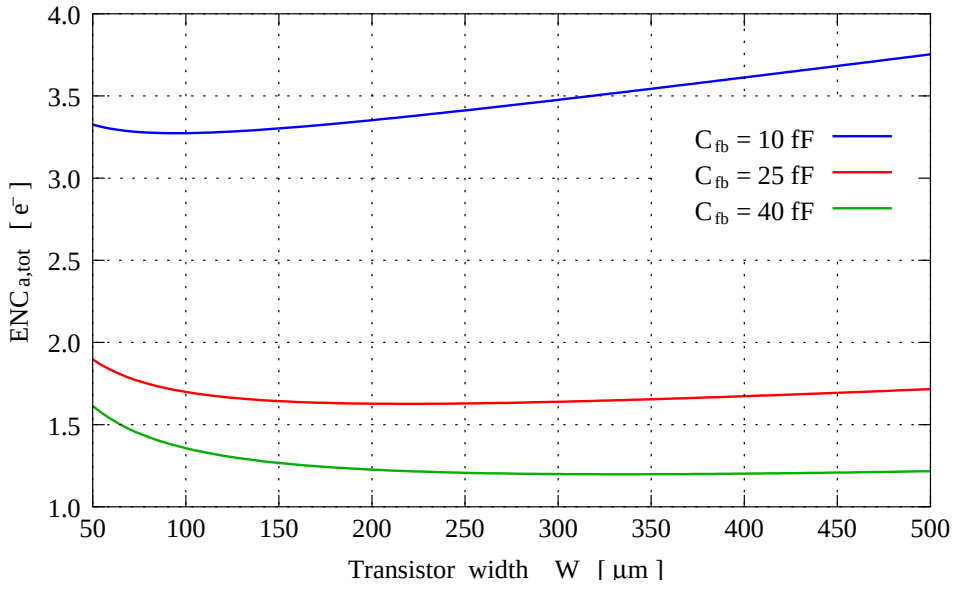


Figure 5.6: Total noise contribution of the feedback amplifier.

Some conclusions can be drawn from the theoretical calculations presented here. Regarding the input transistor, the amplifier contribution to the total noise is minimized by choosing the maximum allowed bias current, the minimum gate length and the gate width around its optimal value W_{opt}. Regarding the feedback network, the noise decreases with the increasing feedback gain G_{fb}, with the increasing feedback capacitance C_{fb}, as well as with the increasing feedback resistance.

5.2 The voltage feedback amplifier

The feedback amplifier configuration is shown in Figure 5.7. C_{in} and C_{fb} are the capacitors in the feedback network, while the reset mechanism is represented by the resistor R_{fb}. The core amplifier is a large gain inverting amplifier.

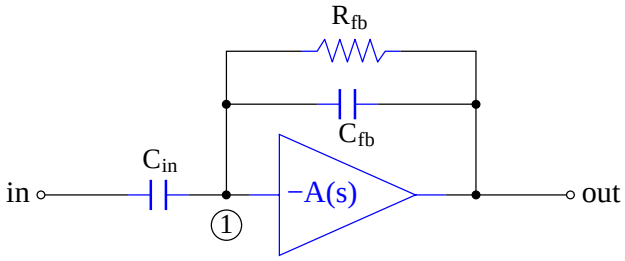


Figure 5.7: Feedback amplifier configuration.

Assume that the core amplifier has the transfer function given by:

$$A(s) = \frac{A_o}{1 + s/p_o} \qquad A_o \gg 1 \tag{5.26}$$

where p_o is the upper 3-dB frequency limit. Assuming that the input impedance is infinitely large and neglecting the output impedance, the voltage transfer function of the feedback configuration $A_{fb}(s) = \frac{v_{out}}{v_{in}}$ can be calculated as follows.

Since the input impedance is infinite, no current flows into the core amplifier. Applying Kirchoff's theorem at the node 1:

$$(v_{in} - v_1)sC_{in} + (v_{out} - v_1)\left(sC_{fb} + \frac{1}{R_{fb}}\right) = 0 \tag{5.27}$$

The voltage at the output node is:

$$v_{out} = -v_1 \cdot A(s) \tag{5.28}$$

Replacing equation 5.28 into equation 5.27, one obtains:

$$A_{fb}(s) = \frac{v_{out}(s)}{v_{in}(s)} \approx -G_{fb} \cdot \frac{s}{s + z_o} \cdot \frac{1}{1 + \frac{s}{p'_o}} \tag{5.29}$$

where

$$\begin{aligned} G_{fb} &= \frac{C_{in}}{C_{fb}} \\ z_o &= \frac{1}{C_{fb}R_{fb}} \\ p'_o &= p_o \frac{A_o}{G_{fb} + 1} \end{aligned} \tag{5.30}$$

In deriving the expression of $A_{fb}(s)$, the approximations $A_o \gg G_{fb}$ and $z_o \ll p_o \ll p'_o$ have been used. G_{fb} is the midband gain of the feedback amplifier, z_o and p'_o are the lower and the upper 3-dB frequency limits of the feedback amplifier bandwidth.

With the numerical values $A_o = 10^5$, $G_{fb} = 100$, $p_o = 10^4 Hz$, $z_o = 10^3 Hz$, the magnitude of $A(s)$ and $A_{fb}(s)$ are plotted in Figure 5.8 as a function of frequency. As a

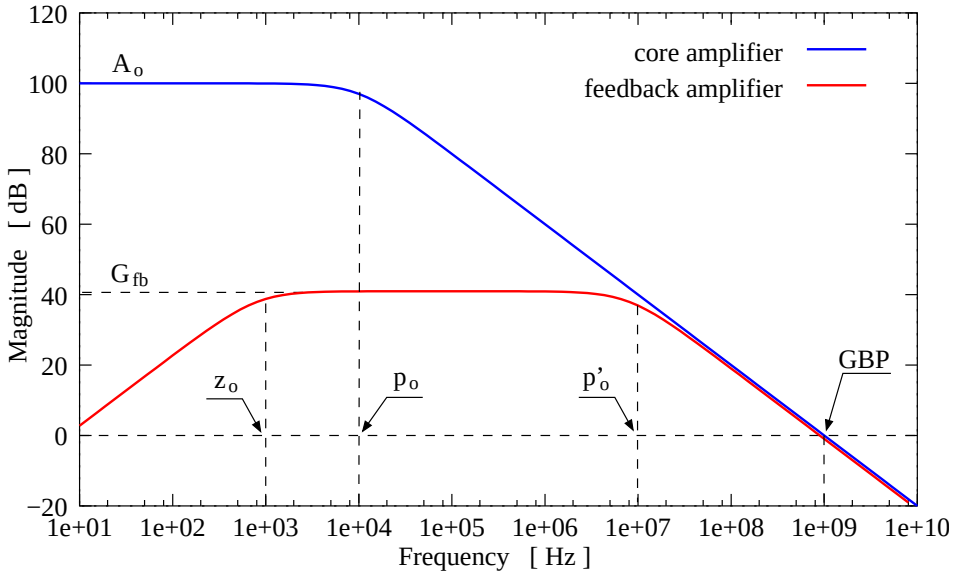


Figure 5.8: Magnitude of the amplifier transfer function

known property of the feedback amplifiers [Sed98], the bandwidth of the feedback amplifier is increased by a factor $A_o/(G_{fb}+1)$, while the gain-bandwidth product GBP[5] remains constant. One can see also that the feedback loop introduces a lower frequency limit $z_o = 1/C_{fb}R_{fb}$ for the feedback amplifier bandwidth.

5.2.1 The effect of the finite input and output impedance on the amplifier transfer function

In the derivation of equation 5.29, it has been assumed that the core amplifier is an ideal voltage amplifier with infinite input impedance and zero output impedance. The influence of the finite input and output impedance on the feedback amplifier characteristics is studied in this sub-section. Figure 5.9 shows the same feedback configuration with the input and output impedance of the core amplifier included. For simplicity reasons, the resistance R_{fb} of the reset mechanism is neglected[6]. Since the input node of the core amplifier is usually the gate of the input MOS transistor, the input impedance is represented by the gate capacitance of this transistor, denoted here by C_{ia}. The output impedance can be considered as a resistor in parallel with a capacitor (i.e. output resistance and load capacitance) and has the expression:

$$Z_{oa} = \frac{R_{oa}}{1+\frac{s}{p_o}} \tag{5.31}$$

where R_{oa} is the output resistance of the amplifier. Notice that p_o in the expression of Z_{oa} is identical to p_o that occurs in the amplifier transfer function $A(s)$ (see equation 5.27);

[5]GBP is defined as the product between the amplifier gain and the upper 3-dB frequency limit

[6]R_{fb} acts only at low frequencies where it sets together with C_{fb} the lower limit of the frequency bandwidth

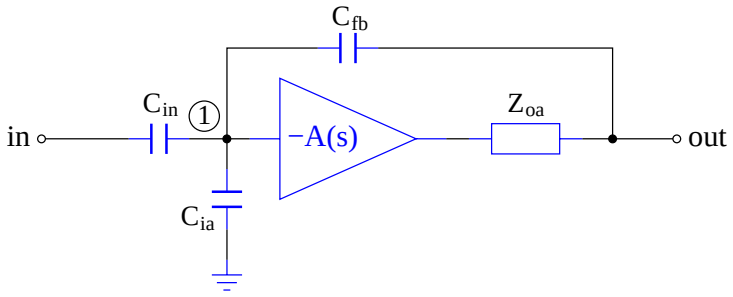


Figure 5.9: Feedback amplifier configuration with finite input and output impedance of the core amplifier.

this is true since the amplifier dominant pole is given by its output resistance in parallel with the load capacitance.

The Kirchoff's equation in the circuit nodes 1 and 2 are:

$$\text{Node 1}: \quad (v_{in} - v_1)sC_{in} + v_1 sC_{ia} + (v_1 - v_{out})sC_{fb} = 0 \tag{5.32}$$

$$\text{Node 2}: \quad v_{out} = -A(s)v_1 + (v_1 - v_{out})sC_{fb}Z_{oa} \tag{5.33}$$

With the substitution of $A(s)$ and $Z_{oa}(s)$, equation 5.33 becomes:

$$v_1 = -v_{out}\frac{1 + s\left(\frac{1}{p_o} + C_{fb}R_{oa}\right)}{A_o - sC_{fb}R_{oa}} \tag{5.34}$$

Replacing v_1 in equation 5.32 leads to:

$$A_{fb}(s) = \frac{v_{out}(s)}{v_{in}(s)} = -G_{fb} \cdot \frac{1 - \frac{s}{z'_o}}{1 + \frac{s}{p''_o}} \tag{5.35}$$

where G_{fb} is the gain factor in equation 5.30 and:

$$\begin{aligned} z'_o &= \frac{A_o}{R_{oa}C_{fb}} \\ \frac{1}{p''_o} &= \frac{1}{A_o C_{fb}}\left[\frac{C_{in} + C_{ia} + C_{fb}}{p_o} + (C_{in} + C_{ia})R_{oa}C_{fb}\right] \end{aligned} \tag{5.36}$$

Comparing the expression of A_{fb} in equation 5.35 with A_{fb} from equation 5.29, one sees that the amplifier gain is the same as in the ideal case. The influence of C_{ia} and R_{oa} can be seen in the frequency dependence. In contrast with the expression 5.29, a zero z'_o is introduced at high frequencies by the finite output resistance R_{oa}. The high frequency pole p''_o is slightly lower than its correspondent p'_o (see equation 5.30) for the ideal case:

$$\frac{1}{p''_o} = \frac{1}{p'_o} + \frac{C_{ia}}{A_o C_{fb} p_o} + \frac{(C_{in} + C_{ia})R_{oa}}{A_o} \tag{5.37}$$

It can be therefore concluded that the finite input and output impedance of the core amplifier influence only the high frequency behavior of the feedback amplifier, the amplifier

gain remaining unaffected.

The next step is to design a core amplifier having a low input noise, large gain (order of $[10^4 \div 10^5]$) and large gain-bandwidth product. It is well known from the literature [Alle02, Bul90] that the large gain requirement is achieved by the cascode stages. Thus, a regulated cascode configuration is chosen for the core amplifier design. The advantages of this configuration over the simple cascode configuration are discussed in the next section.

5.3 Regulated cascode amplifier

The regulated cascode (RGC) amplifier configuration [Säc90] is shown in Figure 5.10. It is composed of two stages: a voltage-to-current amplifier consisting of the transistor T_1 (common-source configuration) with the bias current source $I_{b,in}$, and a current-to-voltage amplifier consisting of the transistors T_2 and T_3 with the bias current sources I_{load} and I_{rgc}. T_1 is the *cascoded* transistor, T_2 is the *cascoding* transistor and T_3 is a feedback transistor

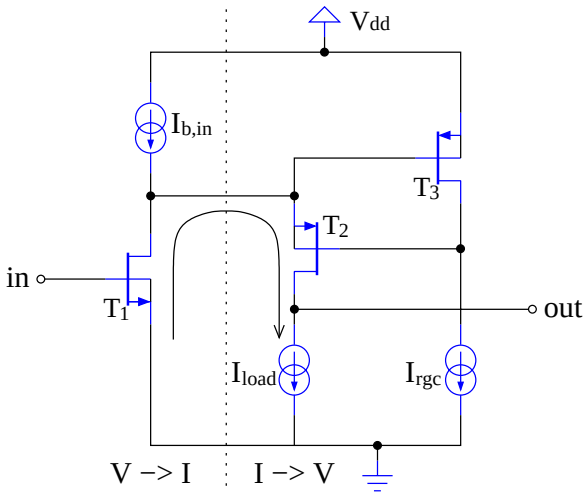


Figure 5.10: Regulated cascode configuration.

that regulates the gate voltage of T_2. The configuration in Figure 5.10 is called *folded* RGC amplifier, since the AC current path circles through both cascoded and cascoding transistor and ground , without going through the positive power supply (the AC current is folded back).

The main difference between the RGC stage and the simple cascode stage arises from the use of T_3. In a simple cascode configuration the gate of T_2 is connected to a fixed potential, while in the RGC configuration the gate voltage of T_2 is regulated by the transistor T_3 such that a constant current is maintained through T_2 event if T_2 is no longer in saturation.

A simple explanation of this effect can be given as follows: assume that the current I_{load} of T_2 decreases for some reasons. Since $I_{b,in}$ is constant, the current through T_1 must

increase and therefore, the drain potential of T_1 increases. One has the following chain effect:
I_{load} decreases $\longrightarrow$ V_{D1} increases $\longrightarrow$ V_{S1} increases $\longrightarrow$ V_{G3} increases $\longrightarrow$ V_{D3} decreases $\longrightarrow$ V_{G2} decreases $\longrightarrow$ large increase of V_{GS2} $\longrightarrow$ large increase of I_{load}.
The "constantness" of the RGC output current is equivalent with a very large output impedance of the RGC stage. It will be seen later on that this regulation mechanism influences also the input impedance of the RGC stage, which will be smaller than for a simple cascode stage.

5.3.1 Low-frequency analysis of the RGC amplifier

The small-signal equivalent circuit of the RGC amplifier at low frequencies (all the capacitances are neglected) is drawn in Figure 5.11 Note that the load current source is

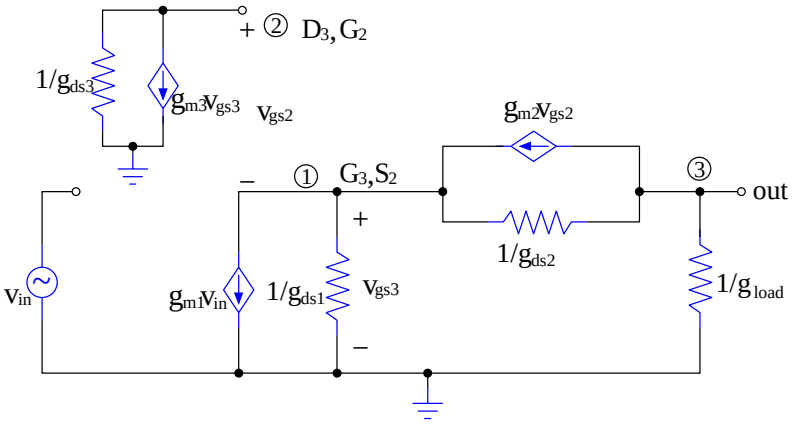


Figure 5.11: Small-signal equivalent circuit of the RGC amplifier.

replaced by its equivalent resistance $1/g_{load}$. The amplifier characteristics such as the voltage gain, input and output impedance are calculated by solving the nodes equations.

Voltage transfer function
Apply the Kirchoff's theorem for currents in the circuit nodes:

$$\begin{aligned} &\text{Node 2}: && (v_{gs2}+v_{gs3})g_{ds3}+g_{m3}v_{gs3}=0 \\ &\text{Node 3}: && v_{out}g_{load}+g_{m2}v_{gs2}+(v_{out}-v_{gs3})g_{ds2}=0 \\ &\text{Node 1}: && g_{m1}v_{in}+v_{gs3}g_{ds1}+(v_{gs3}-v_{out})g_{ds2}-g_{m2}v_{gs2}=0 \end{aligned} \tag{5.38}$$

From the first two equations:

$$\begin{aligned} v_{gs2} &= -v_{gs3}\left(1+\frac{g_{m3}}{g_{ds3}}\right) \\ v_{gs3} &= v_{out}\frac{g_{load}+g_{ds2}}{g_{ds2}}\cdot\frac{1}{1+\frac{g_{m2}}{g_{ds2}}\left(1+\frac{g_{m3}}{g_{ds3}}\right)} \end{aligned} \tag{5.39}$$

Replacing the above expressions in equation 5.38, one obtains the low-frequency voltage gain:

$$A_o = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{load} + \frac{g_{load}+g_{ds2}}{g_{ds2}} \cdot \frac{g_{ds1}}{1+\frac{g_{m2}}{g_{ds2}}\left(1+\frac{g_{m3}}{g_{ds3}}\right)}} \tag{5.40}$$

Although the expression of A_o looks quite complex, it can be simplified by making some assumptions:

- $\frac{g_m}{g_{ds}} \gg 1$ for each transistor ($\frac{g_m}{g_{ds}}$ is the transistor intrinsic gain);
- $g_{load} \ll g_{ds2}$, (e.g. I_{load} is a cascode current source).

Equation 5.40 becomes now:

$$A_o = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{load} + \frac{g_{ds1}}{\frac{g_{m2}}{g_{ds2}}\frac{g_{m3}}{g_{ds3}}}} \tag{5.41}$$

Since $\frac{g_m}{g_{ds}} \gg 1$, one can assume that $\frac{g_{ds1}}{\frac{g_{m2}}{g_{ds2}}\frac{g_{m3}}{g_{ds3}}} \ll g_{load}$. A_o is then:

$$A_o \approx -\frac{g_{m1}}{g_{load}} = -g_{m1}R_{load} \tag{5.42}$$

The amplifier gain is thus given by the transconductance of the first transistor multiplied by the impedance of the load current source. To achieve a high gain, the first transistor must have large g_m (large W/L ratio and large bias current) and the load current source has to be designed with a large output impedance (i.e. cascode current source).

Output impedance of the RGC stage

The circuit for calculating the output impedance of the RGC stage is shown in Figure 5.12. The load current source at the output is replaced by a voltage source v_{out}; no

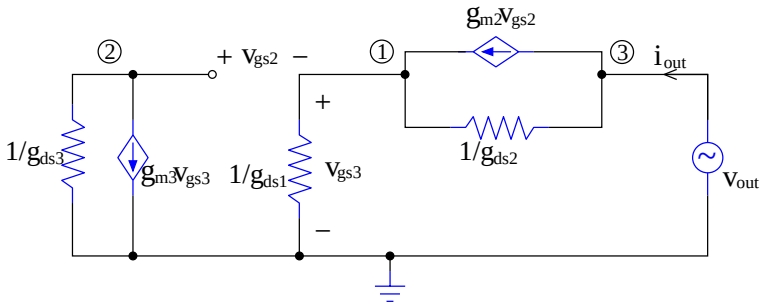


Figure 5.12: Small-signal equivalent circuit for calculating the RGC output impedance.

signal is applied to the input transistor (replaced by its output impedance $1/g_{ds1}$). The Kirchoff's equations in the circuit nodes are:

$$\begin{aligned} &\text{Node 2}: && (v_{gs2}+v_{gs3})g_{ds3} + g_{m3}v_{gs3} = 0 \\ &\text{Node 1}: && v_{gs3}g_{ds1} = g_{m2}v_{gs2} + (v_{out}-v_{gs3})g_{ds2} \\ &\text{Node 3}: && i_{out} = g_{m2}v_{gs2} + (v_{out}-v_{gs3})g_{ds2} \end{aligned} \tag{5.43}$$

Solving for v_{gs2} and v_{gs3} in the first two equations and replacing into the third one, the output impedance is given by:

$$R_{out}^{rgc} = \frac{v_{out}}{i_{out}} = r_{ds1}\left[1 + \frac{g_{ds1}}{g_{ds2}} + \frac{g_{m2}}{g_{ds2}}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)\right] \tag{5.44}$$

where $r_{ds1} = 1/g_{ds1}$ is the output impedance of T_1. With the assumption $\frac{g_m}{g_{ds}} \gg 1$, equation 5.44 becomes:

$$R_{out}^{rgc} \approx r_{ds1}\left(\frac{g_{m2}}{g_{ds2}}\right)\left(\frac{g_{m3}}{g_{ds3}}\right) \tag{5.45}$$

The output impedance of the RGC stage is thus given by the output impedance of the cascoded transistor T_1 multiplied by the intrinsic gain factors of T_2 and T_3. When the load current source is also considered, the total output impedance is:

$$R_{out} = R_{out}^{rgc} \parallel R_{load} \tag{5.46}$$

where $R_{load} = 1/g_{load}$.

Input impedance of the RGC stage

Another important parameter is the input impedance of the RGC stage. This is the impedance seen by the transistor T_1 when "looking" into the source of T_2. The circuit for calculating the RGC input impedance is shown in Figure 5.13. Transistor T_1 is replaced

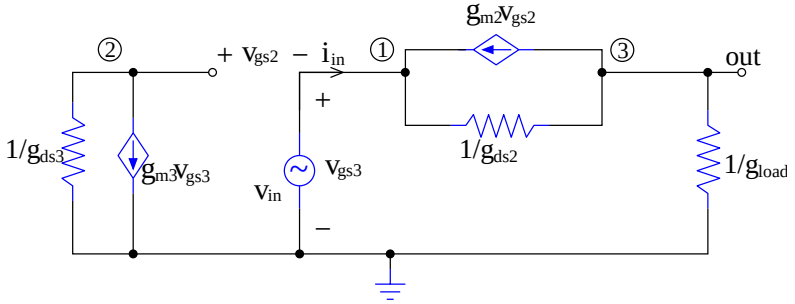


Figure 5.13: Small-signal equivalent circuit for calculating the RGC input impedance.

by a voltage source v_{in} and the current i_{in} is determined from the node equations:

$$\begin{aligned}
&\text{Node 2}: \quad (v_{gs2} + v_{gs3})g_{ds3} + g_{m3}v_{gs3} = 0 \\
&\text{Node 1}: \quad i_{in} = -g_{m2}v_{gs2} + (v_{gs3} - v_{out})g_{ds2} = 0 \\
&\text{Node 3}: \quad v_{out}g_{load} = -g_{m2}v_{gs2} + (v_{gs3} - v_{out})g_{ds2} = i_{in}
\end{aligned} \tag{5.47}$$

Note that $v_{gs3} = v_{in}$; solving for v_{gs2} and v_{out} in the first two equations and replacing them in the third one, the input impedance of the RGC stage is given by:

$$R_{in}^{rgc} = \frac{v_{in}}{i_{in}} = \frac{R_{load} + r_{ds2}}{1 + \frac{g_{m2}}{g_{ds2}}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)} \approx \frac{R_{load}}{\left(\frac{g_{m2}}{g_{ds2}}\right)\left(\frac{g_{m3}}{g_{ds3}}\right)} \tag{5.48}$$

The input impedance of the RGC stage is thus given by the output load resistance divided by the intrinsic gain factors of T_2 and T_3. The voltage gain of the input transistor $g_{m1}R_{in}^{rgc}$ is drastically reduced and so the Miller effect [Sed98] induced by the gate-drain capacitance of T_1.

The small-signal parameters of the regulated cascode amplifier are summarized in Table 5.1, in comparison to the similar parameters of a single transistor stage (common source configuration) and of a simple cascode amplifier. One can immediately observe

Parameter	Single transistor	Cascode amplifier	RGC amplifier
Intrinsic gain ($g_{load} = 0$)	$\frac{g_{m1}}{g_{ds1}}$	$\frac{g_{m1}}{g_{ds1}} \cdot \frac{g_{m2}}{g_{ds2}}$	$\frac{g_{m1}}{g_{ds1}} \cdot \frac{g_{m2}}{g_{ds2}} \cdot \frac{g_{m3}}{g_{ds3}}$
Output impedance	r_{ds1}	$r_{ds1} \cdot \frac{g_{m2}}{g_{ds2}}$	$r_{ds1} \cdot \frac{g_{m2}}{g_{ds2}} \cdot \frac{g_{m3}}{g_{ds3}}$
Input impedance	-	$\frac{R_{load}+r_{ds2}}{\frac{g_{m2}}{g_{ds2}}}$	$\frac{R_{load}+r_{ds2}}{\frac{g_{m2}}{g_{ds2}} \cdot \frac{g_{m3}}{g_{ds3}}}$

Table 5.1: Small-signal parameters of different amplifier stages

the advantages that arise from the use of a RGC amplifier configuration.

5.3.2 High-frequency analysis of the RGC amplifier

It is very important to know the high-frequency behavior of the core amplifier employed in a feedback configuration, since it tends to oscillate if the phase margin is not large enough [Alle02]. A detailed treatment of the high-frequency analysis of the regulated cascode amplifier is performed in Appendix A. The amplifier has a complex frequency behavior, its frequency-dependent transfer function having three poles and three zeros. The required phase margin is achieved by adding a compensation capacitance to the gate-drain capacitance of T_2 (see Figure 5.14). As a side-effect the amplifier bandwidth decreases.

5.3.3 Final design of the core amplifier

The complete schematics of the core amplifier is shown in Figure 5.14 The RGC amplifier output is buffered by the transistor T_4 operating in a source-follower (SF) configuration. The load current source is realized as a high-swing cascode configuration [Cra92] and is formed by the transistors T_{1b2} and T_{2b2}. The bias current sources for T_1, T_3 and T_4

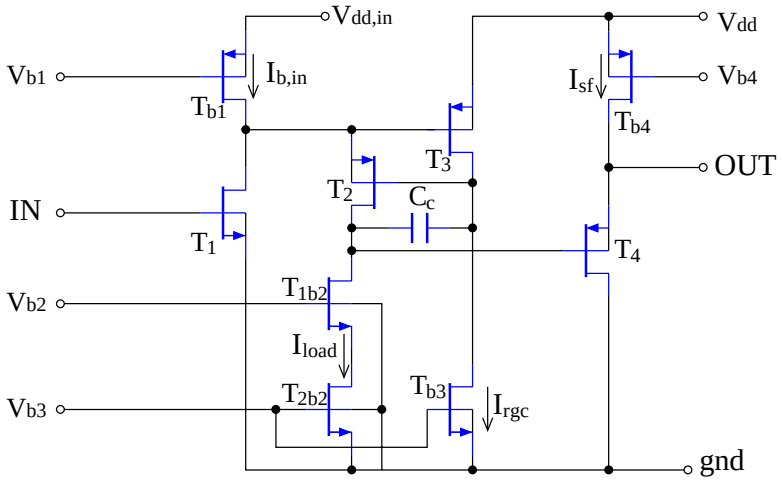


Figure 5.14: Complete schematics of the core amplifier.

are realized as single transistor current sources. The the design parameters of all the transistors as well as the the bias current values are listed in Table C.2 in appendix C.

Since the bias current of the input transistor T_1 is relatively high (large g_{m1} for low noise), the power consumption can be reduced by reducing the voltage drop on the bias transistor T_{b1}. The source of T_{b1} is therefore connected to a separate voltage $V_{dd,in}$ which can be set lower than the global V_{dd}. Figure 5.15 shows the DC analysis of the circuit performed with the SPICE[7] simulator, for two different values of $V_{dd,in}$ ($V_{dd} = 3V$). It

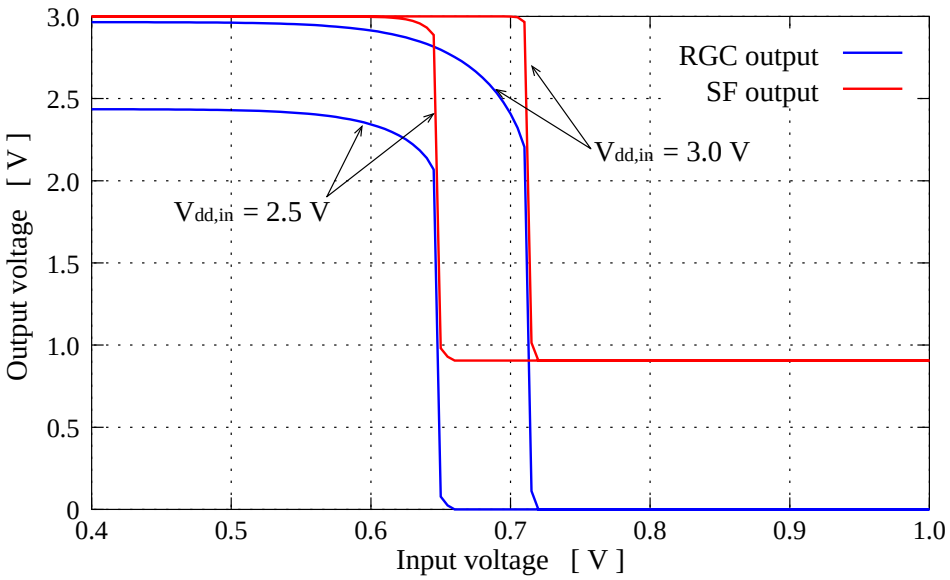


Figure 5.15: Output voltage as a function of the input voltage.

can be seen that the dynamic output range (SF output) is unaffected by the choice of

[7]Simulator Program with Integrated Circuit Emphasis

$V_{dd,in} < V_{dd}$. For $V_{dd} = 3V$ and $I_{b,in} = 40\mu m$, the minimum value of $V_{dd,in}$ is about 2.3V (i.e. $\approx 25\%$ less power).

Regarding the AC analysis of the circuit in SPICE, Figure 5.16 shows the magnitude and the phase shift of the voltage transfer function plotted as a function of frequency. The transfer function is plotted with and without the the compensation capacitance C_c. By adding the capacitance C_c the phase margin is improved at the price of shortening

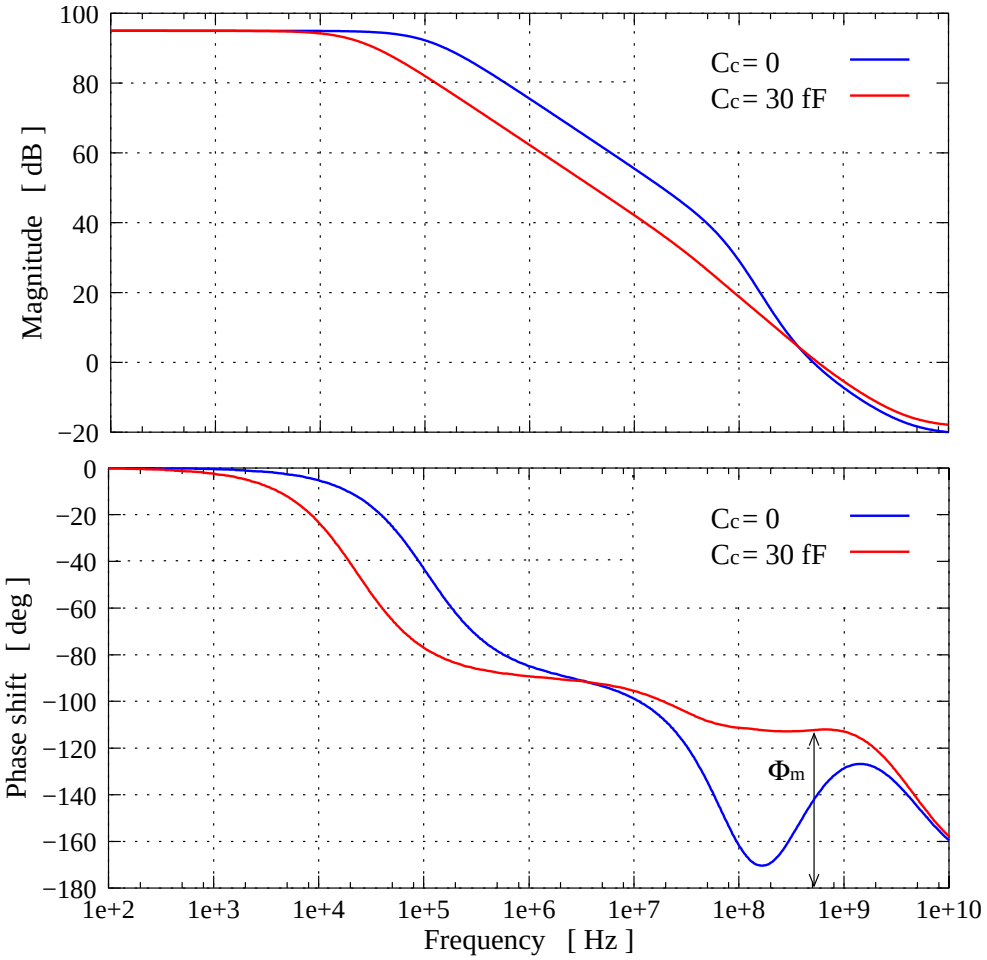


Figure 5.16: Magnitude and phase shift of the transfer function as a function of frequency.

the frequency bandwidth. The amplifier has a low-frequency gain of about 95 dB with the gain-bandwidth product of 1.3 GHz for $C_c = 30fF$. With this capacitance value, the phase margin Φ_m is about 65^o.

The results of the SPICE simulation of the amplifier noise performance are shown in Figure 5.17 The spectral density of the equivalent input noise voltage is plotted as a function of frequency. The flicker noise component dominates at low frequency, while the thermal noise plays a role at frequencies larger than 1 MHz. One can see that the equivalent input noise is dominated by the noise of the input transistor.

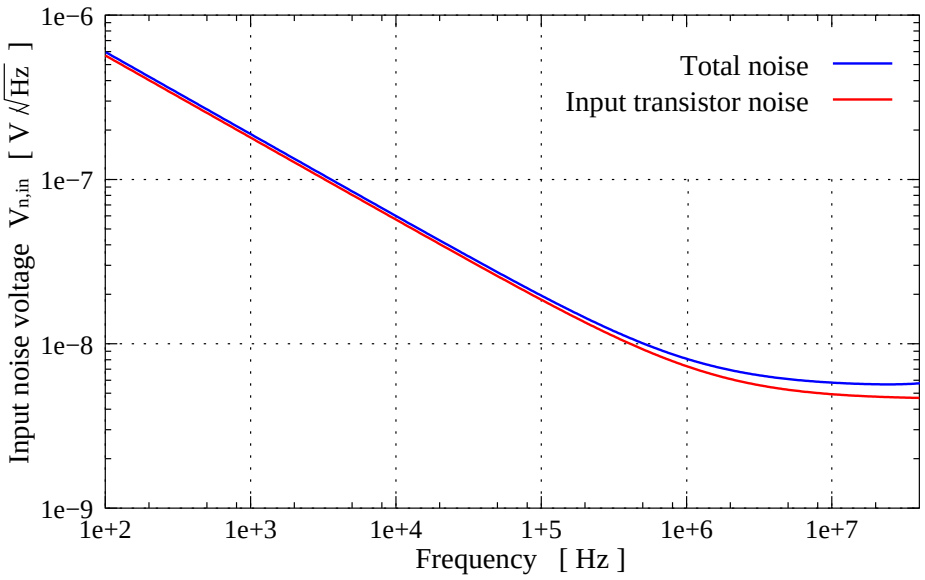


Figure 5.17: Equivalent input noise voltage of the amplifier.

5.4 The complete design of the feedback amplifier

The complete schematics of the amplifier with the feedback network is shown in Figure 5.18 The feedback amplifier gain is given by the ratio of the capacitances in the feedback

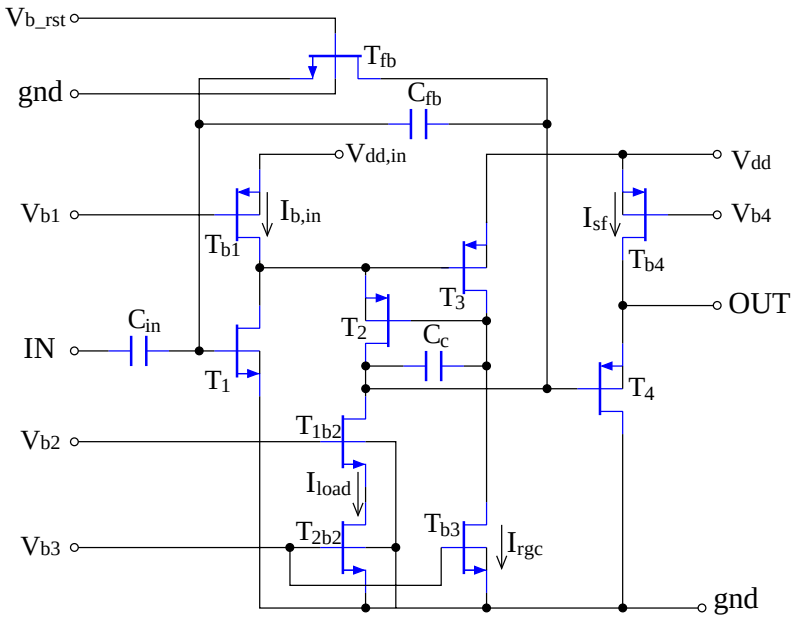


Figure 5.18: Complete schematics of the feedback amplifier.

network and is set to $C_{in}/C_{fb} = 20$.

The amplifier reset mechanism is represented by the NMOS transistor T_{fb} biased in

the subthreshold region [Vit77]. When no signal is applied to the amplifier input, there is no current flowing though T_{fb}. The source potential is equal to the drain potential and the transistor is in the linear region of operation. Hence, T_{fb} is equivalent with a resistance[8] controlled by its gate voltage $V_{b,rst}$. Figure 5.19 shows the magnitude of the feedback gain plotted as a function of frequency for different values of $V_{b,rst}$. The lower

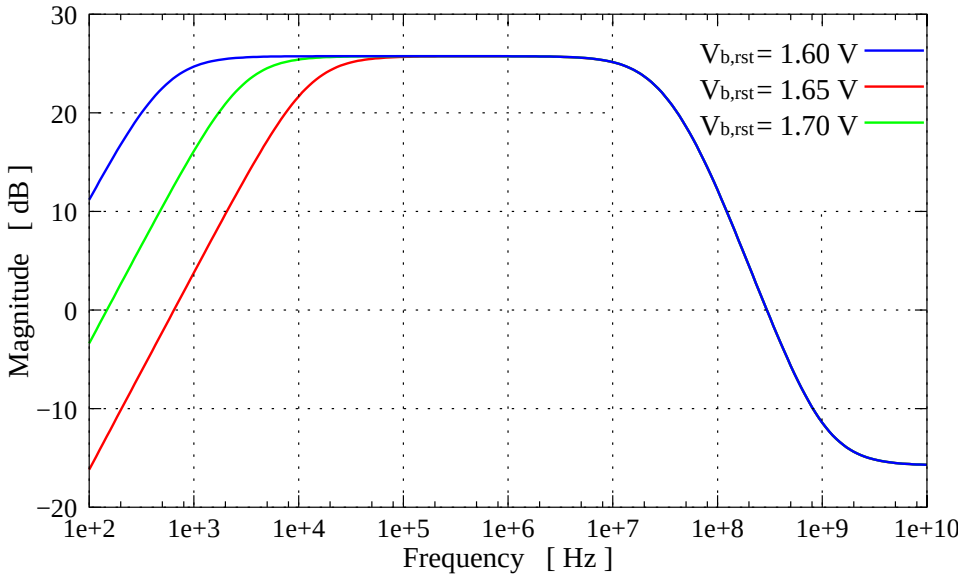


Figure 5.19: Magnitude of the feedback transfer function.

limit of the frequency bandwidth (z_o in equation 5.30) increases with the increasing $V_{b,rst}$ (the equivalent resistance R_{fb} decreases).

If a negative voltage step is applied to the input, the amplifier responds with a positive voltage change. The drain voltage of the feedback transistor increases and T_{fb} reaches the saturation region. The feedback transistor is equivalent now with a constant current source which will discharge the feedback capacitor at a constant rate. Figure 5.20 shows the transient response (i.e. in time domain) of the amplifier to an input voltage step of $-10mV$. One can see that the amplifier output decreases linearly in time, with the slope proportional to the constant current of the feedback transistor: $\frac{dV_{out}}{dt} = \frac{I_{fb}}{C_{fb}}$.

The layout of the feedback amplifier is shown in Figure 5.21. The largest transistor T_1 ($L = 0.6\mu m$, $W = 76.8\mu m$) is realized as a parallel connection [Bak98] of six transistors, each one with the width $W = 12.8\mu m$. The placement of the transistor within the layout is optimized and the effective gate-source and gate-drain capacitance values are reduced[9].

The capacitances in the feedback network C_{in} and C_{fb} are surrounded by guard rings. This layout technique allows a better precision (better matching between capacitors in different pixels) and isolate the capacitors from the substrate noise [Bak98].

[8] In the sub-threshold region, the equivalent resistance is very large (i.e in $G\Omega$ range)

[9] Two adjacent transistors share the same drain (source)

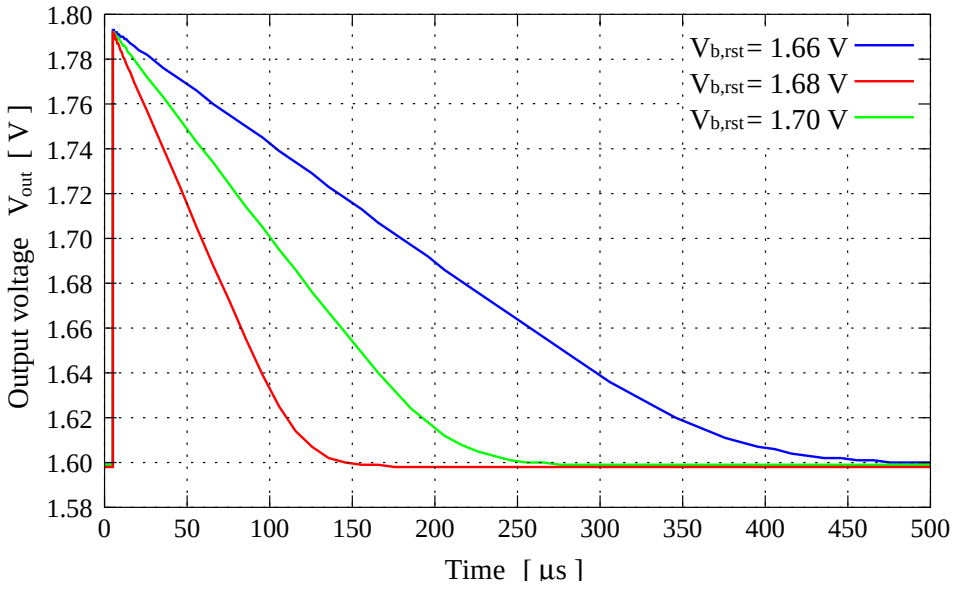


Figure 5.20: Transient response of the amplifier.

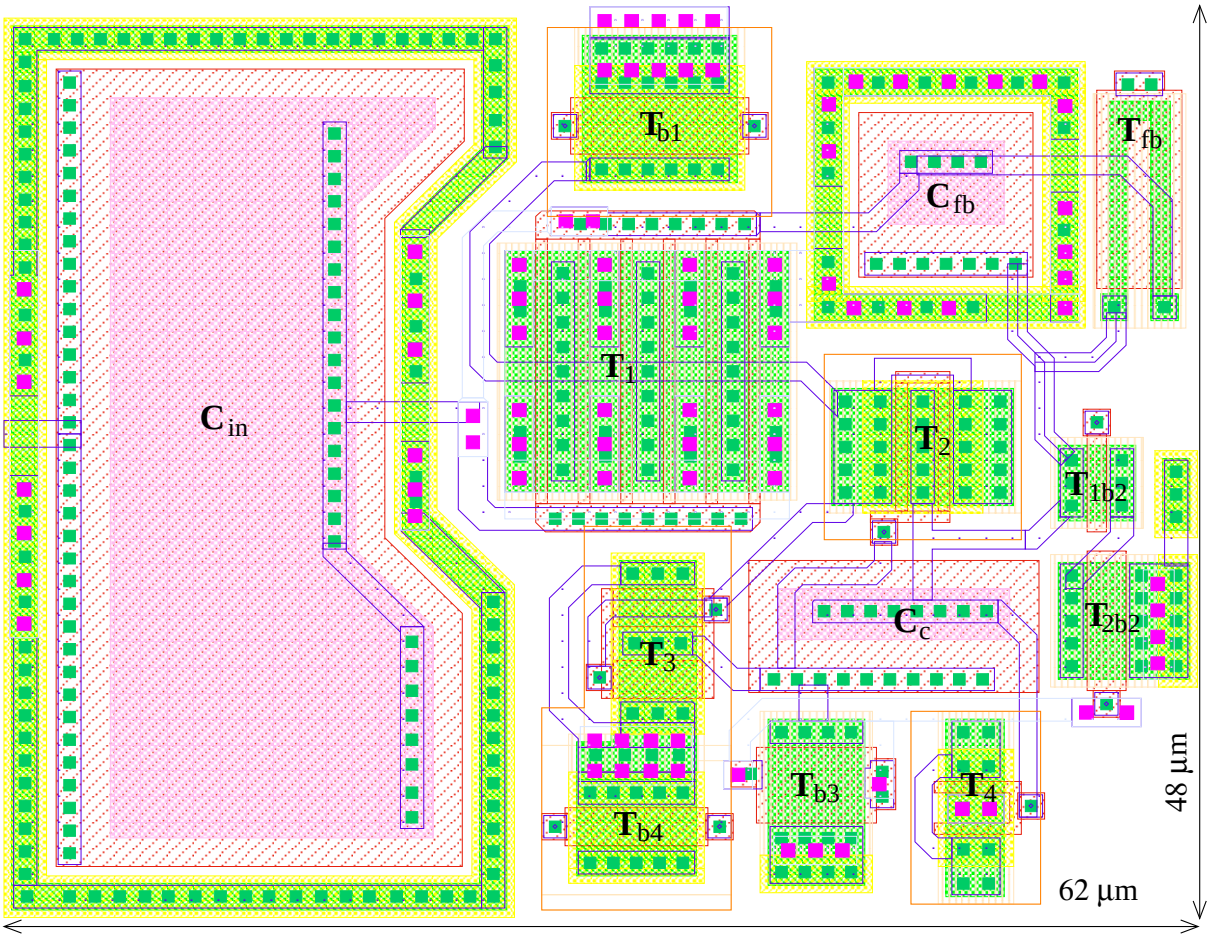


Figure 5.21: Layout of the feedback amplifier.

5.5 Shaper design

In a detector readout system, the signal produced by the amplifier in response to an input charge is usually fed into a filter. The main task of the filter is to reduce the noise of the system by selecting the appropriate frequency bandwidth over which the noise is integrated. Furthermore, the filter aims to transform the amplifier signal from a step-like response to a smooth signal pulse avoiding the effect of pulse overlap or pileup. The maximum of the pulse is the measure of the detector input charge. The filter is called also pulse shaper.

5.5.1 Noise considerations

The most popular type of shaper that is used in particle detection systems is the so-called *semi-gaussian* (S-G) shaper (an approximation of the ideal shaper form derived in [Rad88]). The shaper consists of a differentiator followed by a certain number of integrators. The number of the integrators gives the order of the shaper. The general form of the transfer function (in s-domain) of a S-G shaper of order n is given by [Cha97]:

$$H(s) = \frac{s\tau}{1+s\tau}\left(\frac{1}{1+s\tau}\right)^n \tag{5.49}$$

where τ is the time constant of the differentiator and the integrators. The response of the shaper to an input step signal (in the time domain) is found by performing the inverse of the Laplace transform of the function $H(s)/s$ and is given by:

$$f(t) = \frac{1}{n!}\left(\frac{t}{\tau}\right)^n e^{-t/\tau} \tag{5.50}$$

$f(t)$ has a maximum at $\tau_{sh} = n\tau$ (found by solving for $f'(t) = 0$) which is given by:

$$f_{max} = f(\tau_{sh}) = \frac{n^n}{e^n \cdot n!} \tag{5.51}$$

τ_{sh} is also called shaping (or peaking) time of the S-G shaper. The time response $f(t)$ normalized to its maximum value is plotted in Figure 5.22 One can see that for large n, the shape of the time response is close to a gaussian function.

As we have seen in section 4.3, the dependence of the equivalent noise charge on the filter characteristics is described by the coefficients A_1, A_2 and A_3 from equations 4.30, 4.38 and 4.39, respectively. These coefficients are calculated for an n-order S-G shaper in Appendix B. Their values for $n = 1, 2, .., 5$ are summarized in Table 5.2.

Coefficient	n=1	n=2	n=3	n=4	n=5
A_1	0.923	1.280	1.556	1.791	1.998
A_2	0.923	0.426	0.311	0.256	0.222
A_3	3.694	3.412	3.320	3.274	3.248

Table 5.2: Values of the coefficients A_1, A_2 and A_3

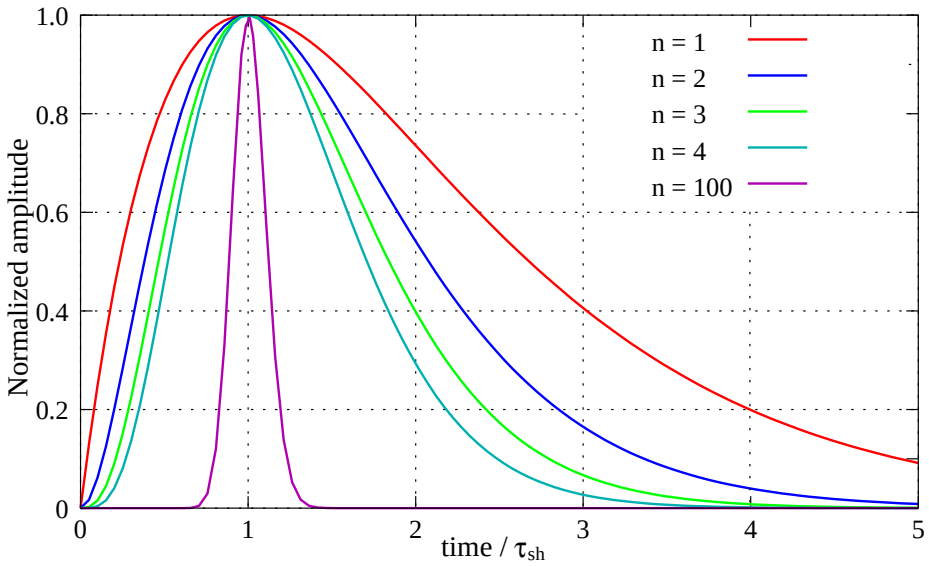


Figure 5.22: Normalized time response of a S-G shaper of order n.

The coefficient A_1 which appears in the noise contribution of all the parallel noise sources (i.e. DEPFET clear current, input noise current of the amplifier) increases with n. The coefficients A_2 (thermal noise) and A_3 (flicker noise) decrease with n. Figure 5.23 shows the total noise of the DEPFET, as well as the noise contribution of the thermal,

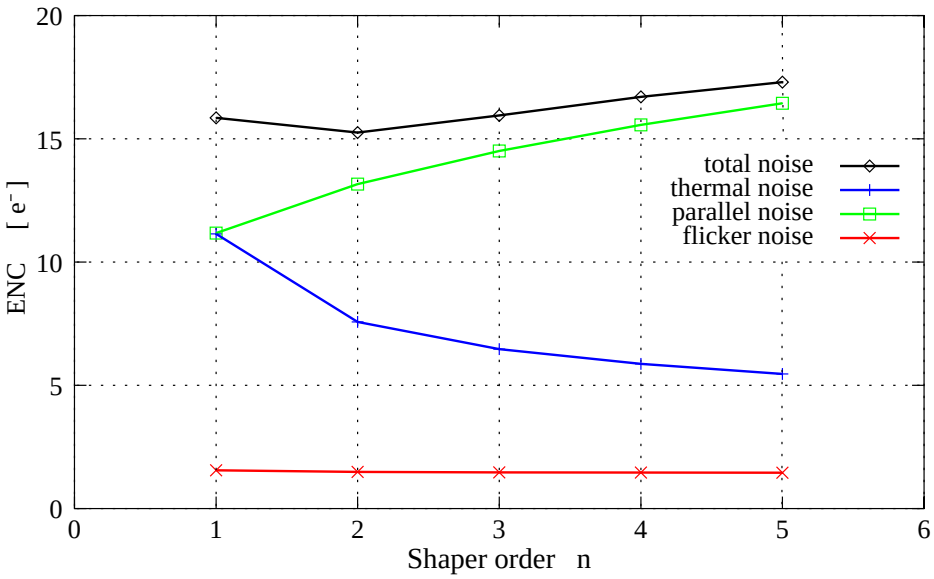


Figure 5.23: Noise contribution as a function of the shaper order n.

parallel and flicker noise sources plotted as a function of the S-G shaper order. For the calculations, we considered the numerical values given at the end of section 4.3. The shaper time constant was taken $\tau = 1\mu s$. One can see that the total noise has a minimum

at $n = 2$, and varies a little with the shaper order.

Since the complexity of the shaper design and hence the needed design area increase almost proportional to the shaper order, a first order S-G has been implemented. Two practical realization of a first order S-G shaper have been developed; they are presented in the next two sub-sections.

5.5.2 CR-RC Shaper

The simplest solution for the realization of a CR-RC is shown in Figure 5.24. The shaper consist of a differentiator stage C_1R_1 followed by an integrator stage R_2C_2. The voltage

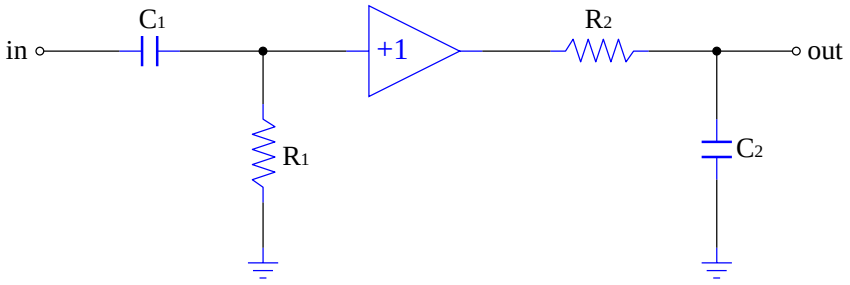


Figure 5.24: Realization of a CR-RC shaper.

transfer function is given by:

$$H(s) = \frac{s\tau_1}{1 + s\tau_1} \frac{1}{1 + s\tau_2} \tag{5.52}$$

where $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$. If C_1, R_1, C_2 and R_2 are chosen such that $\tau_1 = \tau_2 = \tau_{sh}$:

$$H(s) = \frac{s\tau_{sh}}{(1 + s\tau_{sh})^2} \tag{5.53}$$

The realization of such a shaper with the CMOS technology is quite difficult for some practical reasons. As we have seen in the theoretical noise calculations, the optimum shaping time is in the μs range. With the given technology, a capacitor of 500 fF occupies an area of about $550\mu^2$. For two capacitors, the needed area is about 6 % of the total area of a pixel in the DEPFET matrix. For this capacitance value, the resistance R must be in the range of $M\Omega$, which is also impractical to be realized within a pixel.

An alternative solution [Haus02] is presented in Figure 5.25. The resistors in the shaper are replaced by diode-connected MOS transistors (T_1 and T_5). The equivalent resistance of a diode-connected transistor is the inverse of its transconductance which can be made very small if the transistor is long and is biased with low current. The bias current $I_{b,sh}$ of T_1 is mirrored via the current mirrors T_1-T_2 and T_3-T_4, such that the same current $I_{b,sh}$ biases the transistor T_5. Applying a positive voltage step at the input node, the signal is at first differentiated by the capacitor C_1 and the transistor T_1. The current through T_1 changes correspondingly; this current change is mirrored to T_5 via the two current mirrors. Finally, the current change is integrated on the parallel connection of T_5 and C_5 and produces the desired voltage pulse shape.

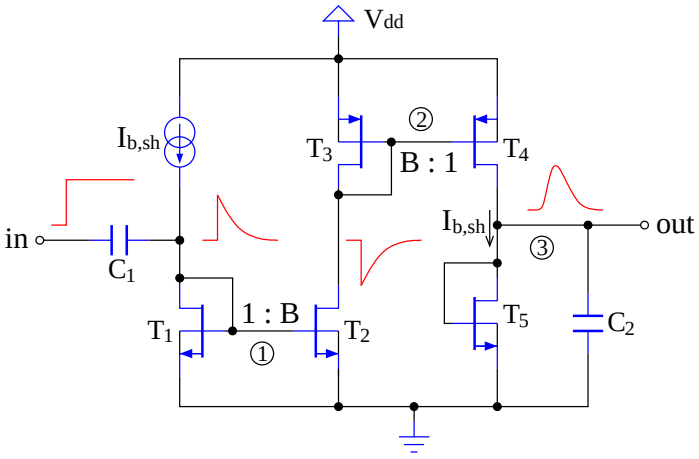


Figure 5.25: Practical realization of a CR-RC shaper in CMOS technology.

The small-signal equivalent circuit of the CR-RC shaper from Figure 5.25 is shown in Figure 5.26 Apart from the gate-source capacitances[10] of T_1 and T_5, all the other

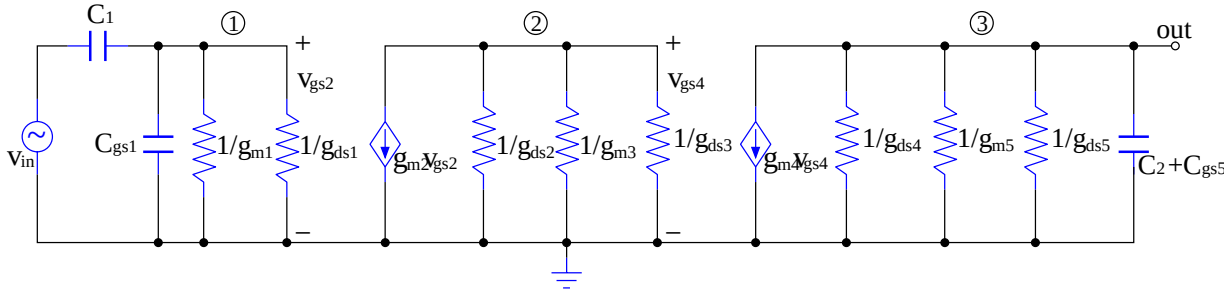


Figure 5.26: Small-signal equivalent circuit of the CR-RC shaper.

transistor capacitances are neglected.

The first part of the circuit forms a voltage divider. The voltage at node 1 is given by:

$$v_1 = v_{in}\frac{\left(\frac{1}{sC_{gs1}} \parallel \frac{1}{g_{m1}} \parallel \frac{1}{g_{ds1}}\right)}{\frac{1}{sC_1} + \left(\frac{1}{sC_{gs1}} \parallel \frac{1}{g_{m1}} \parallel \frac{1}{g_{ds1}}\right)} = v_{in}\frac{sC_1}{g_{m1} + s(C_1 + C_{gs1})} \tag{5.54}$$

where the approximation $g_{m1} \gg g_{ds1}$ has been used. The voltage at the node 2 is:

$$v_2 = -g_{m2}v_{gs2}\left(\frac{1}{g_{m3}} \parallel \frac{1}{g_{ds3}}\right) = -v_1\frac{g_{m2}}{g_{m3}} \tag{5.55}$$

The voltage at the output node is given by:

$$v_{out} = -g_{m4}v_{gs4}\left(\frac{1}{g_{m5}} \parallel \frac{1}{g_{ds4}} \parallel \frac{1}{g_{ds5}} \parallel \frac{1}{s(C_5 + C_{gs5})}\right) = -v_2\frac{g_{m4}}{g_{m5} + s(C_2 + C_{gs5})} \tag{5.56}$$

[10]These capacitances are significantly large, since T_1 and T_5 are long transistors

From the three equations above, the shaper transfer function is found to be:

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{sC_1}{g_{m1} + s(C_1 + C_{gs1})} \frac{g_{m2}}{g_{m3}} \frac{g_{m4}}{g_{m5} + s(C_2 + C_{gs5})} \tag{5.57}$$

With the notations:

$$\tau_1 = \frac{C_1 + C_{gs1}}{g_{m1}} \qquad \tau_2 = \frac{C_2 + C_{gs5}}{g_{m5}} \tag{5.58}$$

the shaper transfer function becomes:

$$H(s) = \frac{g_{m2}}{g_{m3}} \frac{g_{m4}}{g_{m5}} \frac{C_1}{C_1 + C_{gs1}} \frac{s\tau_1}{1 + s\tau_1} \frac{1}{1 + s\tau_2} \tag{5.59}$$

If the bias conditions, the transistors T_1 and T_5 and the size of C_1 and C_2 are chosen such that $\tau_1 = \tau_2 = \tau_{sh}$:

$$H(s) = G_{sh} \frac{s\tau_{sh}}{(1 + s\tau_{sh})^2} \quad \text{with} \quad G_{sh} = \frac{g_{m2}}{g_{m3}} \frac{g_{m4}}{g_{m5}} \frac{C_1}{C_1 + C_{gs1}} \tag{5.60}$$

G_{sh} is the shaper gain.

The shaper is designed for an adjustable shaping time in the range $[1\mu s \div 3\mu s]$. The transistor dimensions and the capacitance values in the CR-RC shaper are listed in Table C.3 in appendix C. The shaping time can be varied by varying the bias current $I_{b,sh}$. Figure 5.27 shows the simulated transient response (with SPICE) of the CR-RC shaper

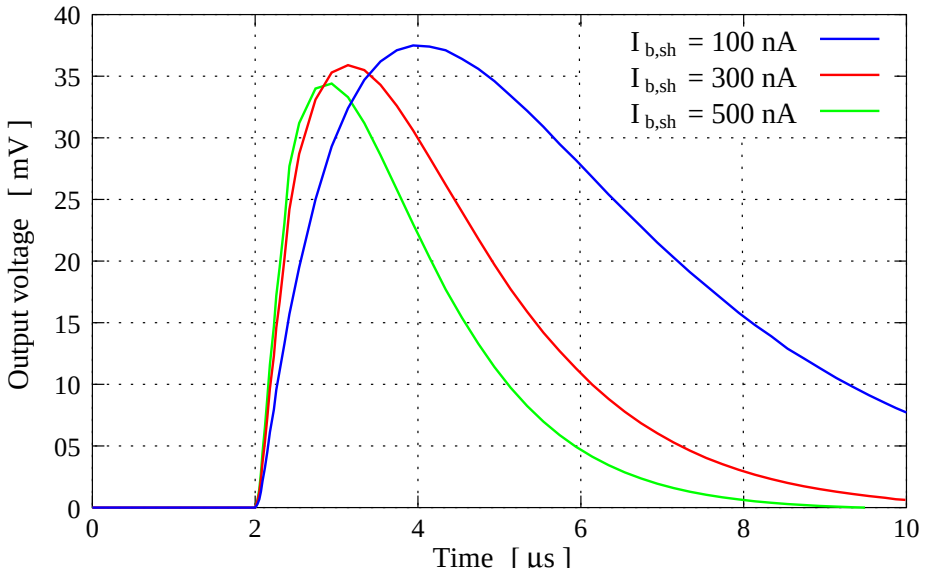


Figure 5.27: Transient response of the CR-RC shaper ($v_{in} = 100mV$).

at different values of the bias current $I_{b,sh}$. The shaper gain varies slightly with bias current.

The layout of the CR-RC shaper is shown in Figure 5.28. It can be seen that the largest design area is occupied by the capacitances C_1 (500 fF) and C_2 (650 fF).

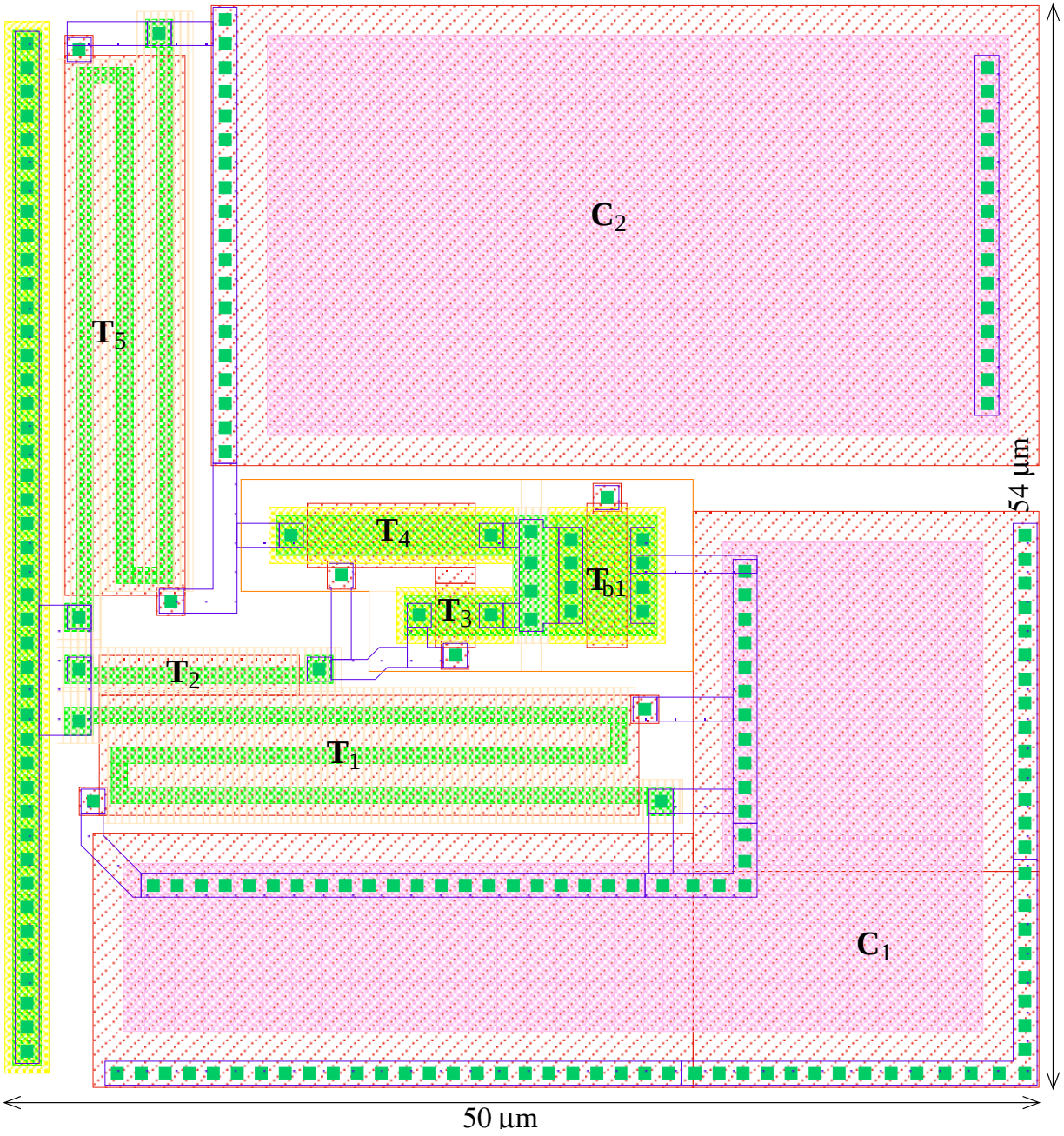


Figure 5.28: Layout of the CR-RC shaper.

5.5.3 S-G shaper based on differential OTA

The basic principle of the shaper based on differential OTA[11] is to combine a differentiator and an integrator, each of them being built with operational transconductance amplifiers of very high output impedance [Ste91].

[11] Operational Transconductance Amplifier

Differentiator based on a differential OTA

The schematics of a differentiating stage based on a differential OTA is shown in Figure 5.29a. The transfer function can be found by analyzing the small-signal equivalent

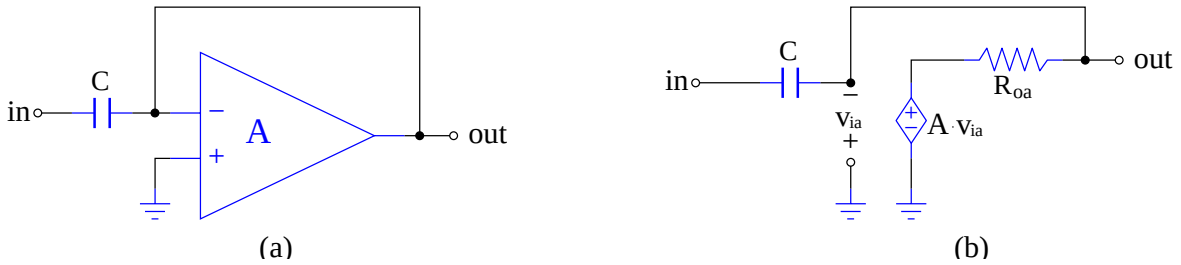


Figure 5.29: Differentiating stage based on OTA.

circuit in Figure 5.29b. The OTA is replaced by its equivalent schematic consisting of a voltage-controlled voltage source $A \cdot v_{ia}$ (A is the open-loop gain) in series with the output impedance R_{oa}. The input impedance of the OTA is assumed to be infinitely large; hence, the current flowing through the capacitor C is equal to the current flowing through R_{oa}:

$$(v_{in} + v_{ia})sC = \frac{v_{out} - A \cdot v_{ia}}{R_{oa}} \tag{5.61}$$

Noting that $v_{out} = -v_{ia}$, the above equation becomes:

$$v_{in}sC = v_{out}\left(sC + \frac{A+1}{R_{oa}}\right) \tag{5.62}$$

and the transfer function is :

$$H_{diff}(s) = \frac{v_{out}}{v_{in}} = \frac{sCR_{of}}{1 + sCR_{of}} \tag{5.63}$$

where $R_{of} = R_{oa}/(A+1)$ is the output impedance with the feedback loop closed. The expression in equation 5.63 is nothing else than the transfer function of a differentiating stage, with the time constant $\tau_d = CR_{of}$.

Integrator based on a differential OTA

The schematics of an integrating stage based on a differential OTA is presented in Figure 5.30a. Performing the similar analysis for the small-signal equivalent circuit in Figure 5.30b, the transfer function is found to be:

$$H_{int}(s) = \frac{v_{out}}{v_{in}} = \frac{1}{1 + sCR_{of}} \tag{5.64}$$

with $R_{of} = R_{oa}/(A+1)$. $H_{int}(s)$ is the transfer function of an integrator.

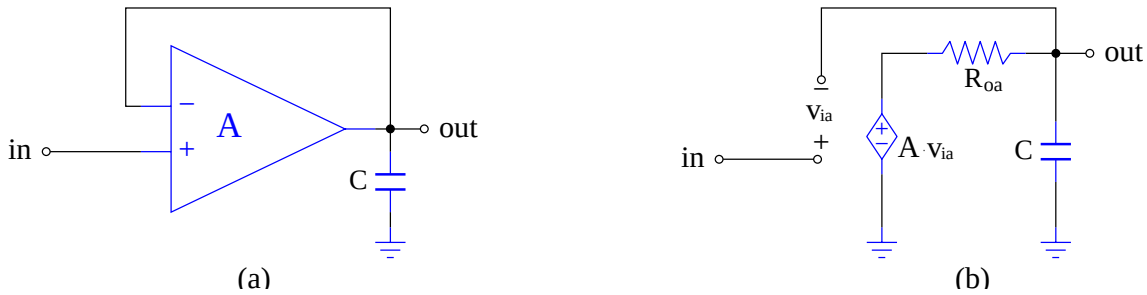


Figure 5.30: Integrating stage based on OTA.

A first order S-G shaper is obtained by combining both stages described before (see Figure 5.31).

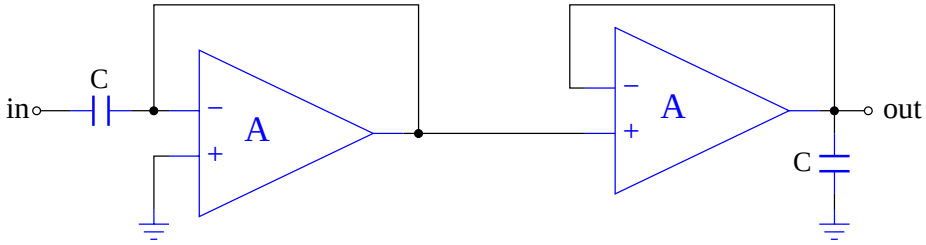


Figure 5.31: S-G shaper based on OTAs.

The shaper transfer function will be given by:

$$H(s) = \frac{s\tau_{sh}}{(1+s\tau_{sh})^2} \quad \text{with} \quad \tau_{sh} = \frac{C \cdot R_{oa}}{1+A} \tag{5.65}$$

A large shaping time (μs) requires that the OTA has very large output impedance and low amplification. These requirements are accomplished by the operational transconductance amplifier shown in Figure 5.32. This configuration is called *symmetrical* OTA configuration (the input stage consisting of T_1, T_2, T_3 and T_4 is symmetrical). The gain of the symmetrical OTA configuration is given by [Lak94]:

$$A_v = \frac{g_{m1}}{B} R_{oa} \quad \text{with} \quad R_{oa} = r_{ds6} \parallel r_{ds8} \tag{5.66}$$

where g_{m1} is the transconductance of T_1 (T_2), B is the current transfer ratio of the current mirrors $T_3 - T_5$ and $T_4 - T_6$; r_{ds6} and r_{ds8} are the output resistances of T_6 and T_8, respectively. The close-loop output impedance which determines the shaper time constant will be given by:

$$R_{of} = \frac{R_{oa}}{1+A_v} \approx \frac{B}{g_{m1}} \tag{5.67}$$

The close-loop output impedance is therefore the inverse of the transconductance of the input transistor multiplied by the current transfer ratio. In comparison with the equivalent

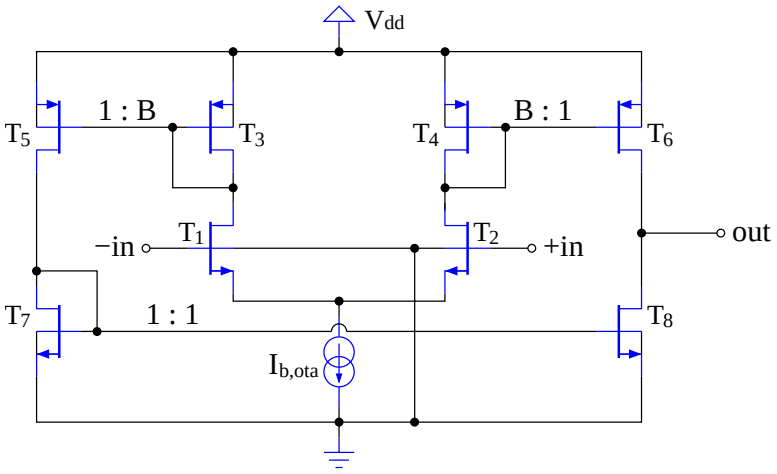


Figure 5.32: Symmetrical OTA configuration.

resistance which enters the time constant in the CR-RC shaper from the previous subsection, and which is given by $1/g_m$, R_{oa} can be further increased by increasing the current gain B. Consequently, larger time constants can be achieved.

Figure 5.33 shows the results of the transient analysis of the shaper based on OTA, for different values of the bias current. As one can see, the value of the shaping time is

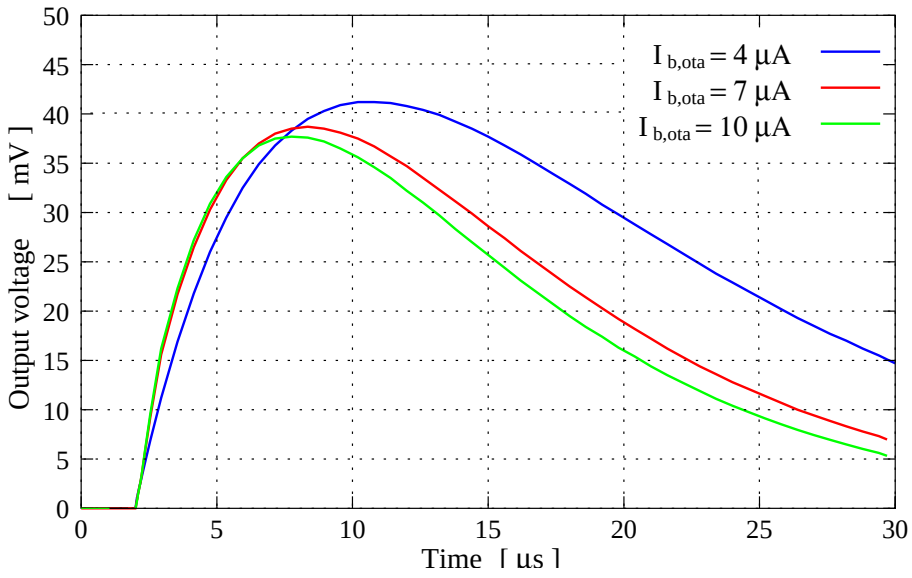


Figure 5.33: Transient analysis of the shaper based on OTAs ($v_{in} = 100mV$).

3 to 4 times larger than in the CR-RC shaper, although the design area of the shaper is only 17 % larger than the area of the CR-RC shaper (see the layout in Figure 5.34). The transistor dimensions and the capacitance values are given in Table C.4 in appendix C.

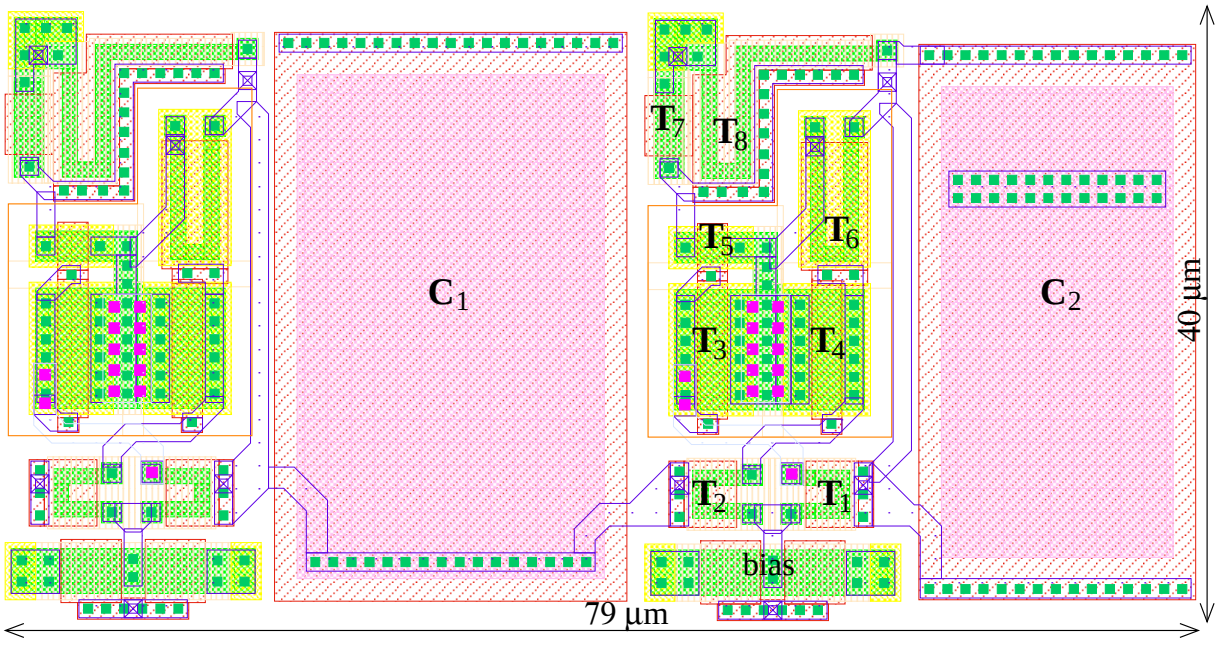


Figure 5.34: Layout of the shaper based on OTAs.

5.6 Analog output buffer

The task of the output buffer is to facilitate the measurement of the output signals of the feedback amplifier or shaper without degradation of the frequency bandwidth. Considering the case of the shaper, an output load capacitance will add directly to the capacitance in the integrating stage and affects drastically the integrator time constant.

The output buffer is realized as a source-follower configuration, as shown in Figure 5.35 T_1 is the transistor connected as source-follower and is biased by a current mirror

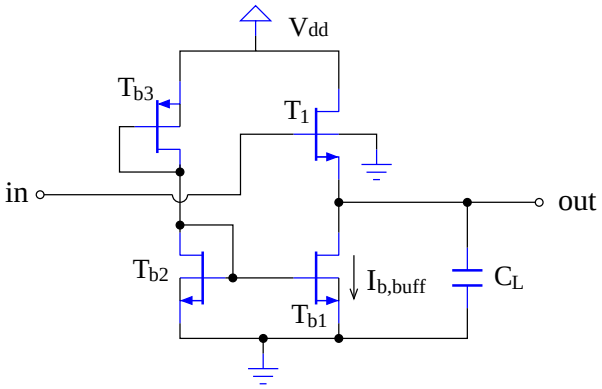


Figure 5.35: Output buffer as source-follower.

consisting of the transistors T_{b1}, T_{b2} and T_{b3}. The upper 3-dB frequency limit of the source

follower is given by [Lak94]:

$$f_{3dB} = \frac{g_{m1}}{C_L} \tag{5.68}$$

where C_L is the output load capacitance (parasitic capacitance of the bonding pad, input capacitance of the oscilloscope probe, etc.) The requirement for the output buffer is that its upper limit of the frequency bandwidth is larger than the feedback amplifier/shaper bandwidth for load capacitance as large as 10 pF.

5.7 Multi-channel structure of the readout

The analog readout consisting of the DEPFET bias source, the feedback amplifier and the shaper is integrated in a multi-channel structure on the electronic chip. The layout of the entire readout structure is shown in Figure 5.36. There are ten readout channels on the chip, five of them with the feedback amplifier and the CR-RC shaper and five with the feedback amplifier and the shaper based on OTA. Since the future goal is to implement the analog readout in a parallel readout matrix for a DEPFET matrix structure, the pitch between two readout channels is taken as the pitch in the DEPFET pixel matrix (i.e 140 μm). Cross-talk effects, differences between channels (i.e. mismatch effects) can be therefore studied.

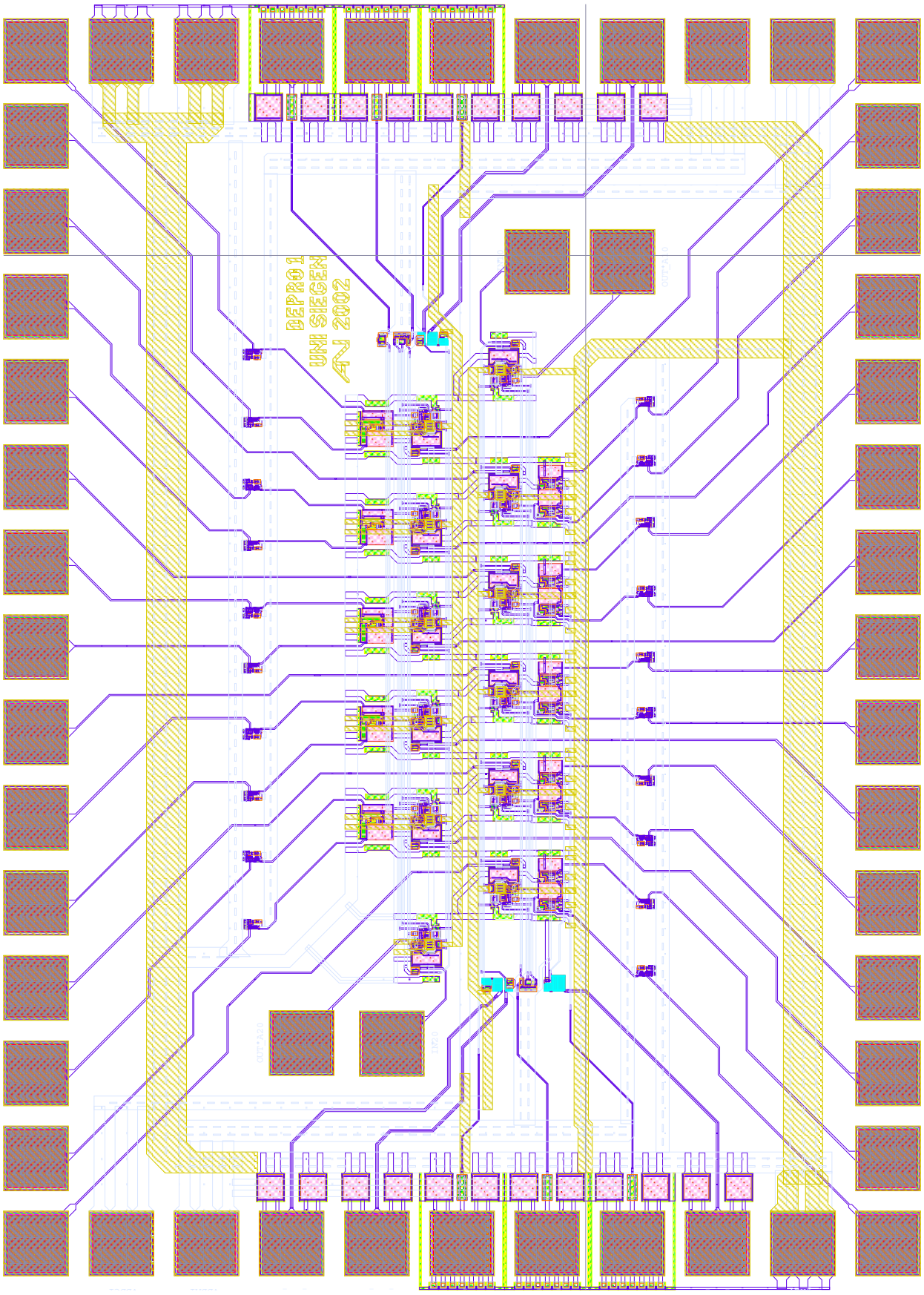


Figure 5.36: Layout of the entire readout chip.

Chapter 6

Measurement of the readout chip without detector

This chapter presents the performances of the readout chip measured without the DEPFET detector. The readout chip has been fabricated in a multi-project wafer run through Europractice IC Service[1] at Austria Micro Systems (AMS). The chip was wire-bonded on a chip carrier in our electronic laboratory.

6.1 Setup for testing the readout

In order to test the readout chip, a dedicated printed circuit board (PCB) was developed. A picture of the PCB is shown in Figure 6.1. The input voltage signal is provided by a pulse generator (HP 81110A); the amplifier and the shaper outputs are visualized with a digital oscilloscope (HP 54825 - Infinium). The bias connector on the PCB provides the bias voltages for V_{dd}, $V_{dd,in}$ and $V_{b,rst}$ (see Figure 5.18), as well as the reference voltages for the current sources[2] needed in the readout circuit.

[1] www.europractice.imec.be

[2] $I_{b,in}$, I_{load}, I_{rgc} and I_{sf} in Figure 5.18, $I_{b,sh}$ in Figure 5.25.

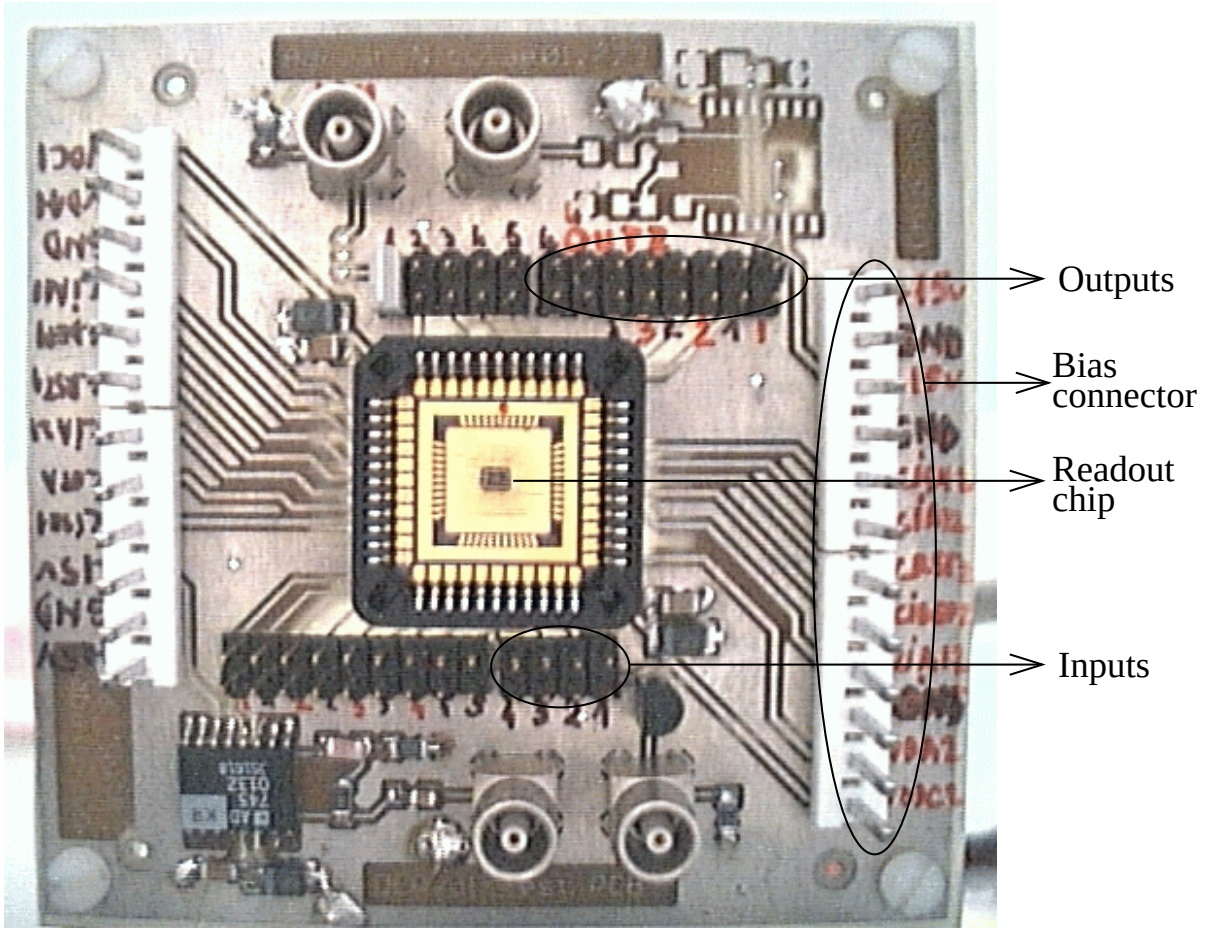


Figure 6.1: PCB for testing the readout chip.

6.2 Measurement of the DEPFET bias current source

The output current of the DEPFET bias current source (see Figure 5.2a) is measured as a function of the output voltage for $V_{dd} = 3V$. Figure 6.2 shows the measured current-voltage characteristics (solid lines) together with the simulated (with SPICE) characteristics (dashed lines). One can see that the measurements are in good agreement with the simulations.

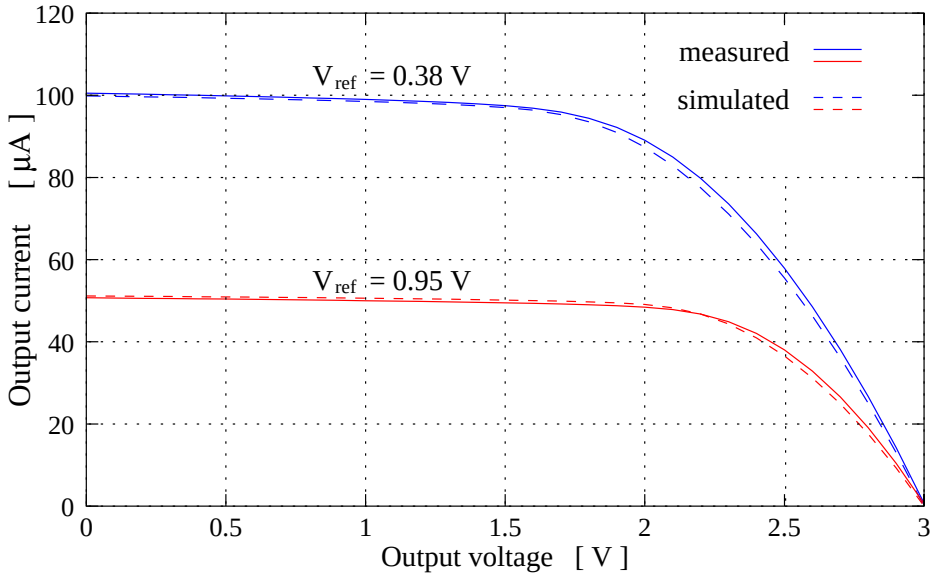


Figure 6.2: Current-voltage characteristics of the DEPFET bias current source.

6.3 Measurement of the feedback amplifier

The measurement of the feedback amplifier characteristics are presented in this section. A negative voltage step from the pulse generator is applied to the input. The output of the amplifier buffer is monitorized with a low-capacity ($< 1pF$) oscilloscope probe.

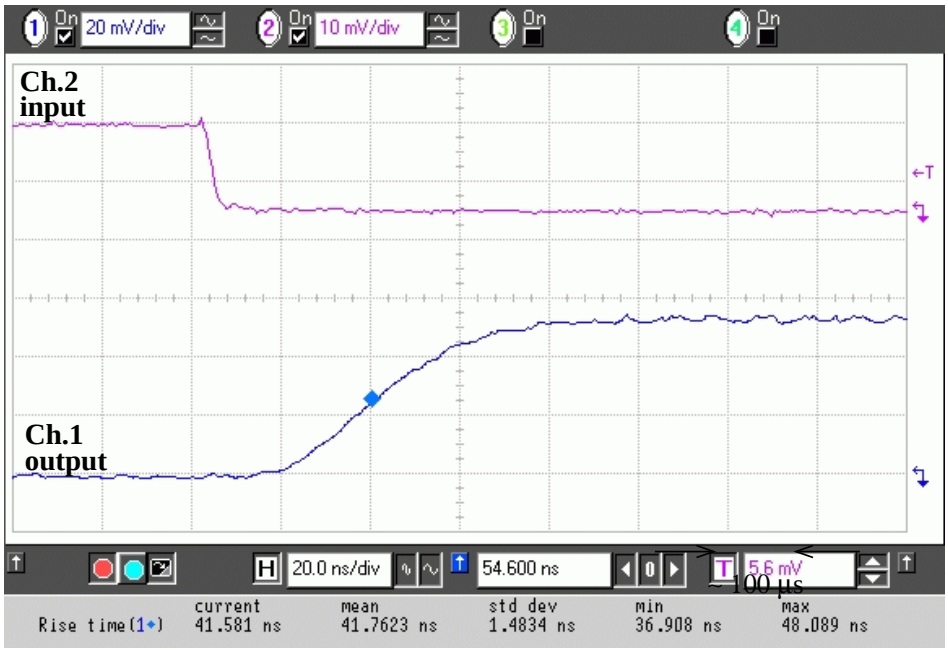


Figure 6.3: Rise time of the amplifier output signal in response to a negative input signal

Figure 6.3 shows the amplifier output signal together with the input signal. A rise time of $41.7 \pm 1.5ns$ is measured, which results in 3-dB frequency limit of about 8.4 MHz. This value is larger than the DEPFET frequency limit of 2 MHz.

The functionality of the reset mechanism - NMOS transistor in sub-threshold regime (T_{fb} in Figure 5.18) - is also tested here. Figure 6.4 shows the amplifier output signal for different values of the gate voltage $V_{b,rst}$ of the feedback transistor. After the out-

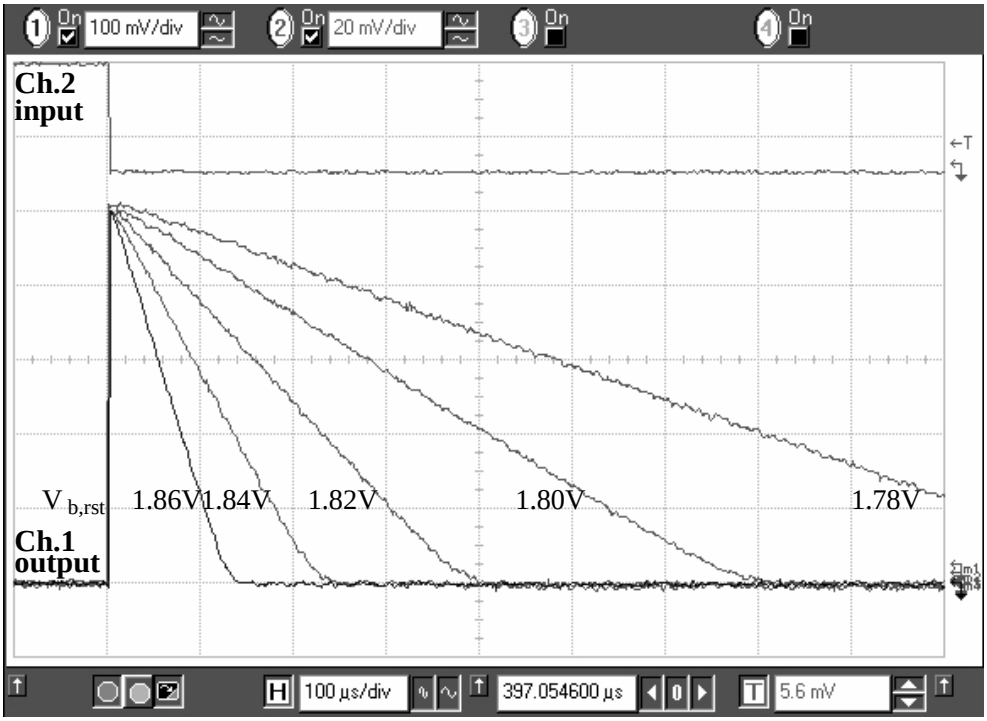


Figure 6.4: Amplifier output signal for different values of the gate voltage of the reset transistor.

put voltage increases to its maximum value, the feedback capacitor is discharged by the constant current in the feedback transistor. Thus, the output voltage decreases linearly with the time. From the slope of the linear decrease (slope $= \frac{I_{fb}}{C_{fb}}$), the discharge current can be calculated. Taking the case $V_{b,rst} = 1.80V$, a discharge current of $\approx 12pA$ is found ($C_{fb} = 25fF$).

The variation of the discharge current in the feedback transistor for different readout channels is also evaluated. These variations are due to variations of the threshold voltage of the input transistor (T_1 in Figure 5.18) as well as the variations of the threshold voltage of the feedback transistor. Figure 6.5 shows the amplifier output voltage of five readout channels at $V_{b,rst} = 1.80V$. The slope of the linear decrease of the amplifier output voltage has a relative variation of about $\pm 7\%$ for all five channels.

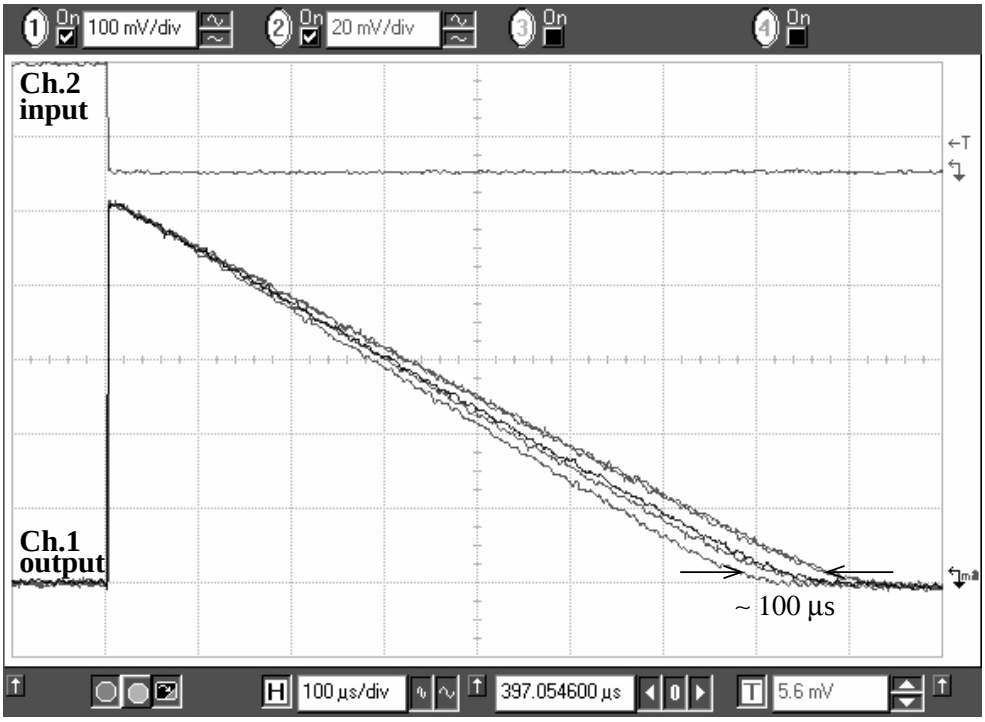


Figure 6.5: Amplifier output signal from five readout channels at $V_{b,rst} = 1.80V$.

6.4 Measurement of the CRRC shaper

The CRRC shaper can not be tested separately, but only together with the amplifier. A small step signal is applied to the amplifier input and the amplifier output becomes the input signal for the CRRC shaper. The shaper output signal goes into the shaper buffer, whose output is monitorized with an oscilloscope probe ($10M\Omega \parallel 9pF$).

The dependence of the shaping time on the shaper bias current ($I_{b,sh}$ in Figure 5.25) is investigated. Figure 6.6 shows the shaper output signal for different values of the bias current. The shaping time varies between 1 and 3 μs.

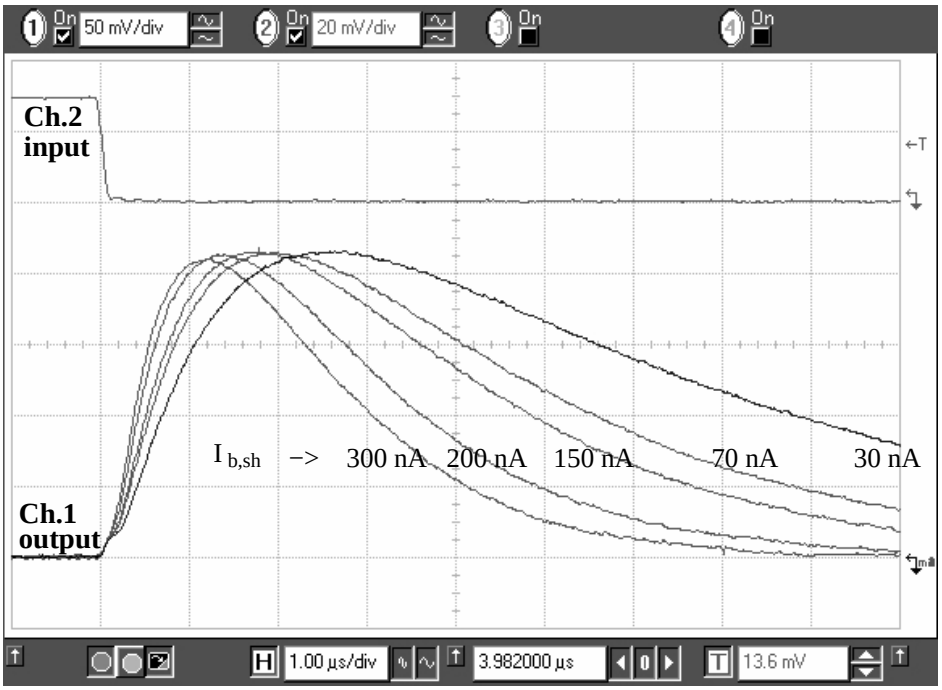


Figure 6.6: Output signal of the CRRC shaper for different values of the shaper bias current.

The uniformity of the shaper output for all five readout channels is also evaluated. The shaper response of all the readout channels for the same input signal is shown in Figure 6.7.

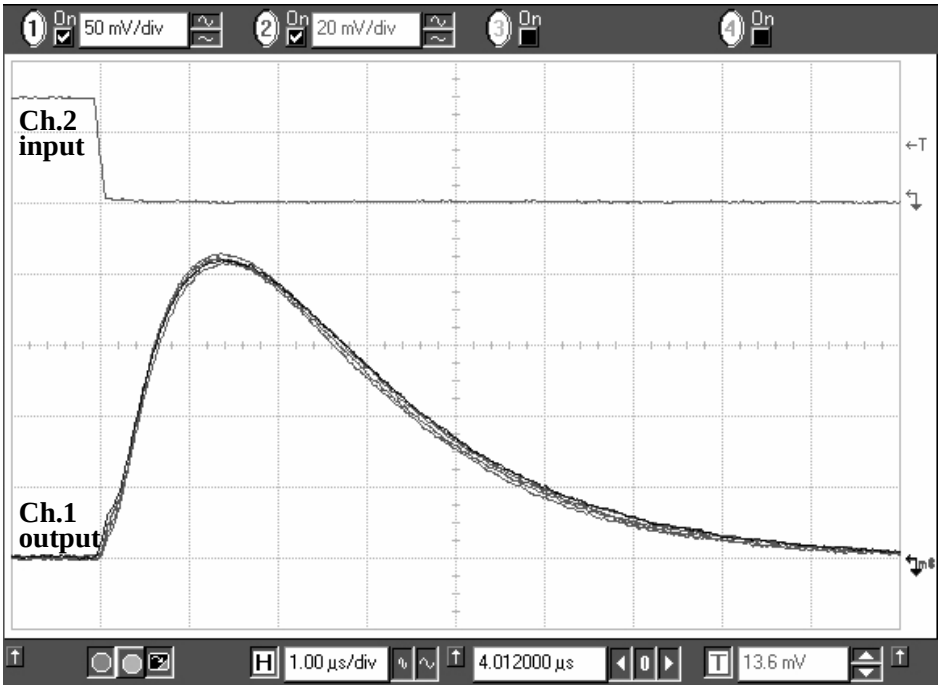


Figure 6.7: Output signal of the CRRC shaper for five readout channels.

One can see no significant differences between different readout channels.

The linearity of the readout system response is also investigated here. Figure 6.8 shows the measured amplitude of the shaper output signal as a function of the amplitude of the amplifier input signal (step signal). The system response is linear for an input voltage

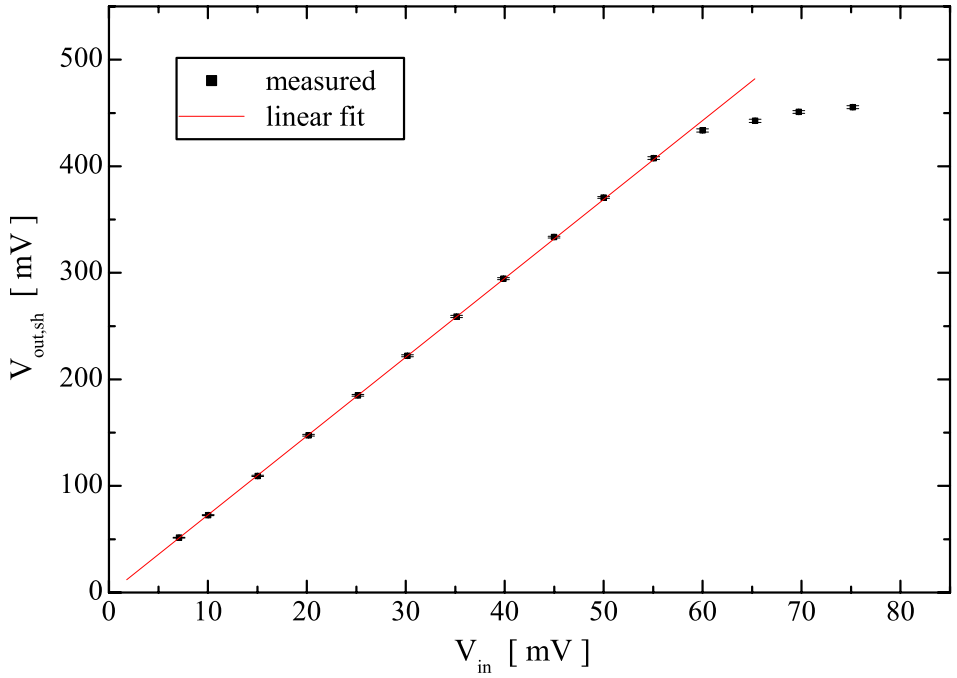


Figure 6.8: Linearity of the amplifier and CRRC shaper response.

range of about 60 mV. From the slope of the straight line fit one obtains the overall amplification of 7.38 ± 0.02. This value is slightly larger than the simulated amplification of 6.85. This difference of approximately 8% stays however within the specifications for the parameter variations[3] in the planar process (10 to 15%).

6.5 Measurement of the shaper based on OTAs

The second version of the shaper (based on operational transconductance amplifier - OTA) which was implemented in the readout chip was also successfully tested. Figure 6.9 shows the shaper output signal for different values of the shaper bias current ($I_{b,ota}$ in Figure 5.32). The shaping time varies between 5 and 13 μs which is about three times larger than the shaping time of the CRRC shaper.

[3]The value of the capacitances in the feedback network of the amplifier can vary within 12%.

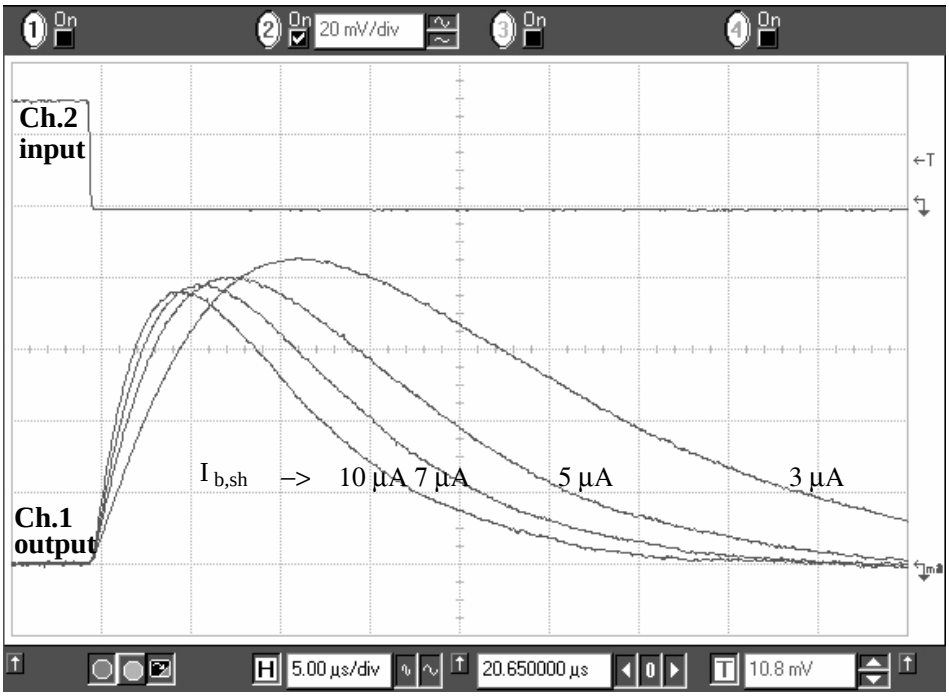


Figure 6.9: Output signal of the OTA shaper for different values of the shaper bias current.

The uniformity of the shaper response of all five readout channel is illustrated in Figure 6.10.

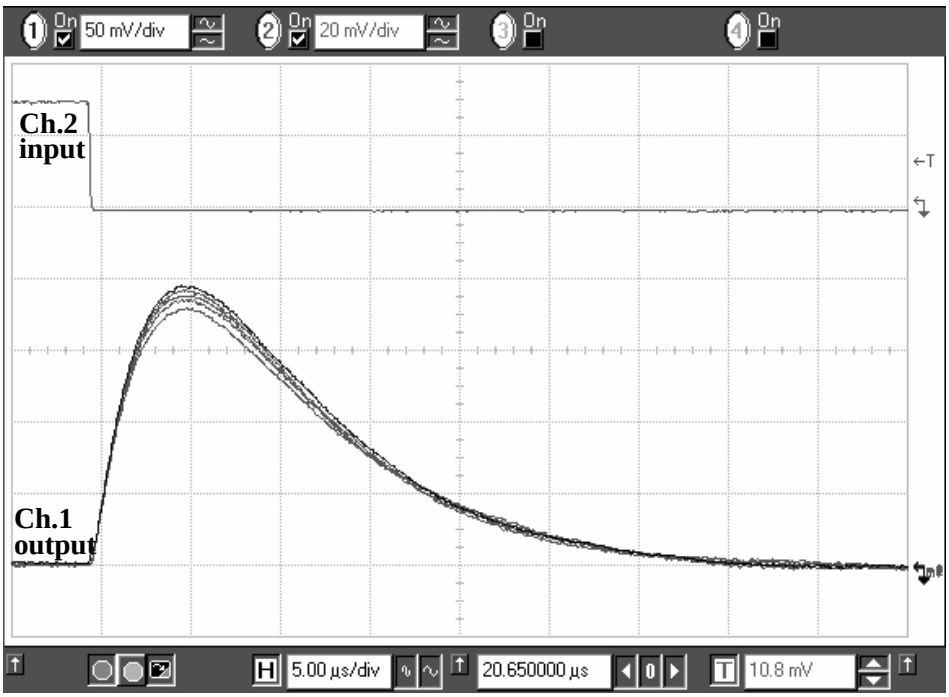


Figure 6.10: Output signal of the OTA shaper for five readout channels.

The shaper output signal is plotted in Figure 6.11 as a function of the amplifier input signal. From the slope of the linear fit, an overall amplification of 6.74 ± 0.02 is found.

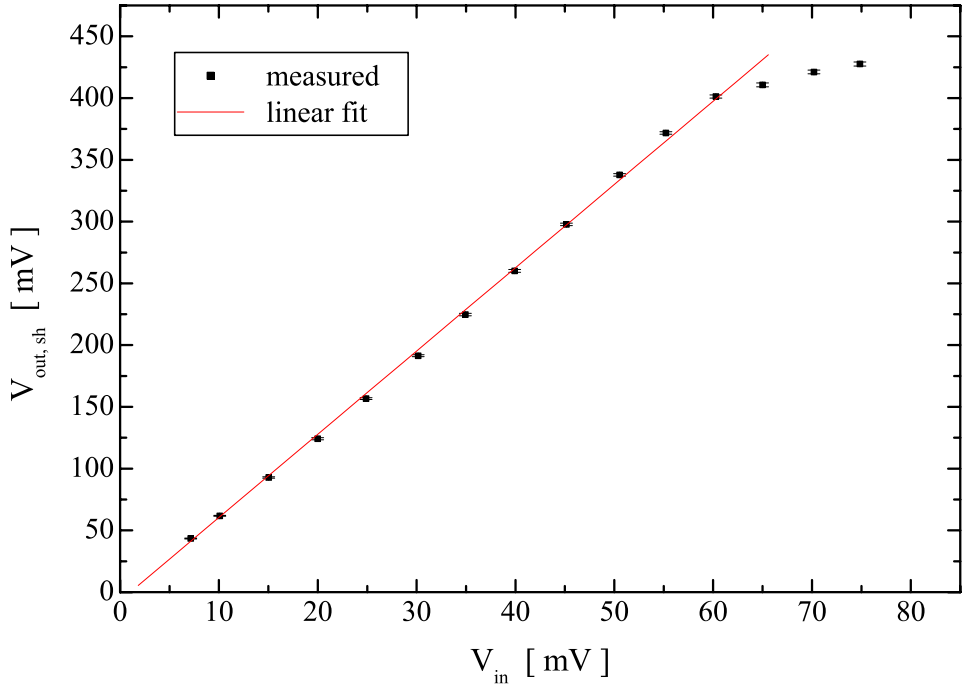


Figure 6.11: Linearity of the amplifier and OTA shaper response.

The simulated amplification factor is 6.54 which is about 3% lower than the measured one.

Since the PCB board used for the measurements presented here is not adequate for low noise measurements (due to stray inductances and capacitances), the readout chip is wire-bonded together with the DEPFET detector on a small hybrid PCB. The total noise of the readout system is evaluated from the measurements of energy spectra from x-ray radioactive sources. The results are presented in the next chapter.

Chapter 7

Measurements of the readout chip with the detector

The noise performances of the DEPFET detector system are evaluated by recording energy spectra from the x-ray radioactive sources ^{55}Fe and ^{109}Cd. The main x-ray lines of these sources are listed in Table 7.1. The errors in the number of *e-h* pairs generated by the

Source	Life time	Peak description	Energy [keV]	No. of *e-h* pairs in Si
^{55}Fe	2.73 y	Mn-K$_\alpha$	5.895	1619.5 ± 14.1
^{55}Fe	2.73 y	Mn-K$_\beta$	6.490	1782.9 ± 15.0
^{109}Cd	462.6 d	Ag-K$_\alpha$	22.103	6072.2 ± 28.1
^{109}Cd	462.6 d	Ag-K$_{\beta_1}$	24.932	6849.5 ± 30.1
^{109}Cd	462.6 d	Ag-K$_{\beta_2}$	25.445	6990.4 ± 30.4

Table 7.1: X-ray energies from ^{55}Fe and ^{109}Cd [Nuc91]

x-ray photons in silicon are determined by the statistical fluctuations in the ionization process (Fano noise).

The energy measurements are performed with new DEPFET structures which are identical to those presented in section 2.5, except that the external gate contact[1] is missing. The reason for that is to minimize the stray capacitance of the internal gate (connected to the external gate via two openings in the JFET channel implant - see Figure 2.14 and 2.15). The charge-voltage signal gain is higher and the noise performance of the detector improves. The JFET operating point is set through the clear contact as explained in section 2.4.1. All the measurements presented in this chapter are performed at room temperature.

[1]This contact is used only for measurements of the static JFET characteristics.

7.1 Setup for energy measurements

The structure containing single DEPFET pixels is placed together with the readout chip on a hybrid PCB (see Figure 7.1), with the view to minimizing the parasitic effects of all the stray inductances and capacitances at the input node. The source of the JFET transistor from the DEPFET detector is connected directly (via a short bonding wire) to the input pad of the readout chip.

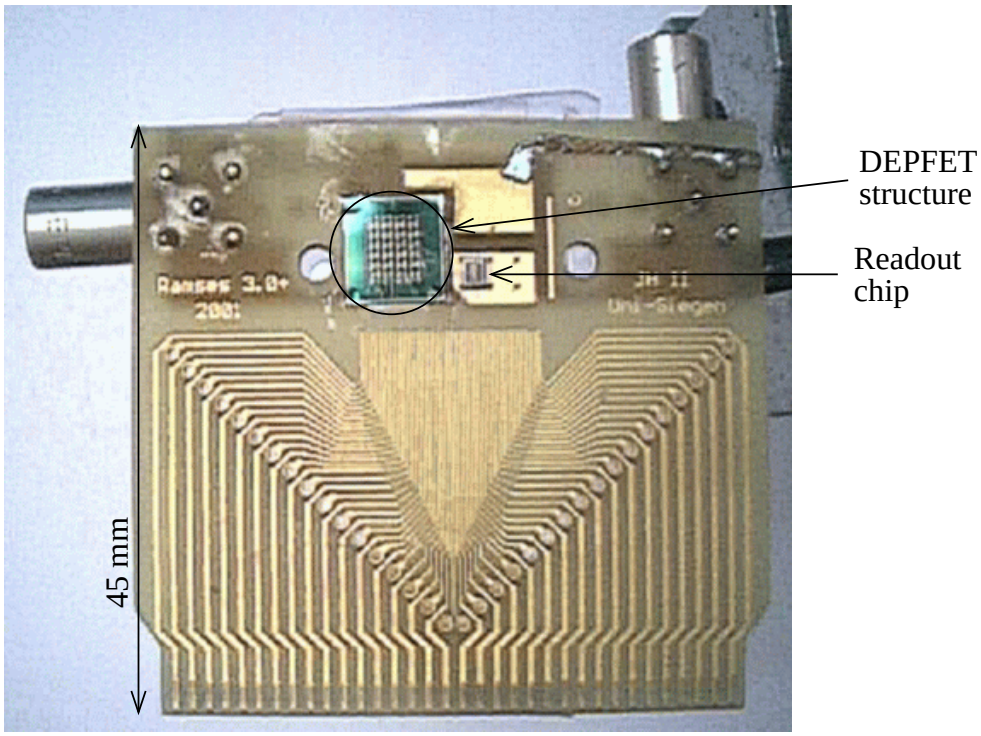


Figure 7.1: Hybrid PCB with DEPFET structure and readout chip.

To provide all the supply voltages for the DEPFET detector and for the readout chip, a dedicated PCB is designed. The supply PCB is foreseen with an edge connector, where the hybrid PCB is plugged in. Figure 7.2 shows a picture of the setup containing the supply PCB with the hybrid PCB plugged in. The setup is placed into a Faraday cage in order to isolate it from electromagnetic pick-up noise.

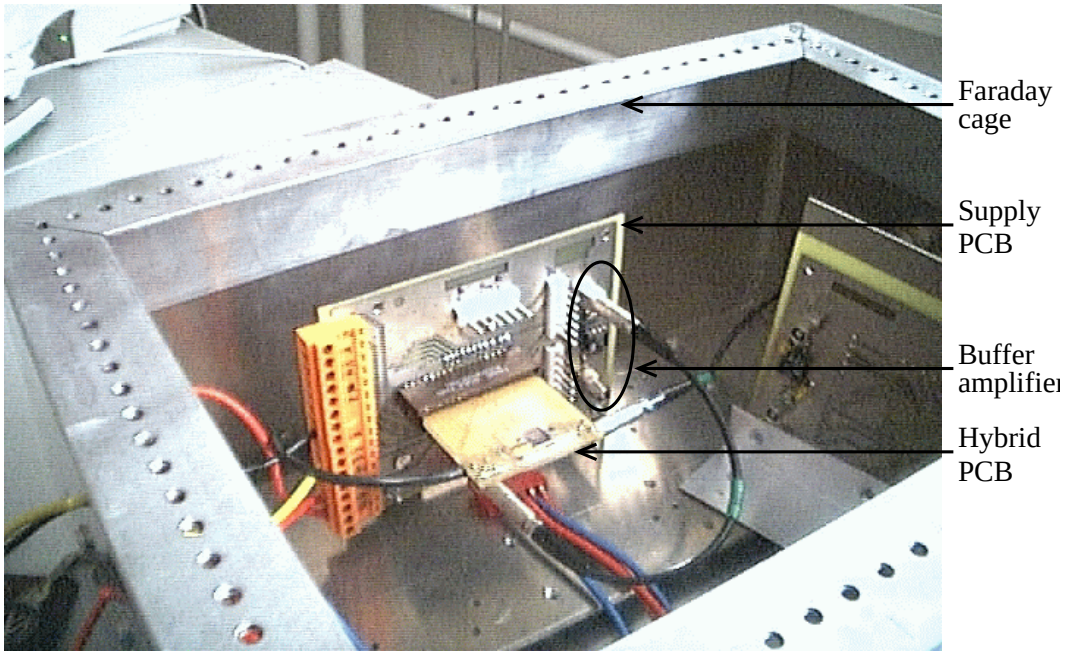


Figure 7.2: Picture of the setup in a Faraday cage.

For recording energy spectra, the shaper output signal must be fed into a Multi Channel Analyzer (MCA). Since the input impedance of the MCA is $1k\Omega$ (small in comparison to the output impedance of the readout circuit), an intermediate buffer amplifier stage is built on the supply PCB. The schematic of the buffer amplifier is shown in Figure 7.3. The amplification factor is set by the resistance ratio R_2/R_1.

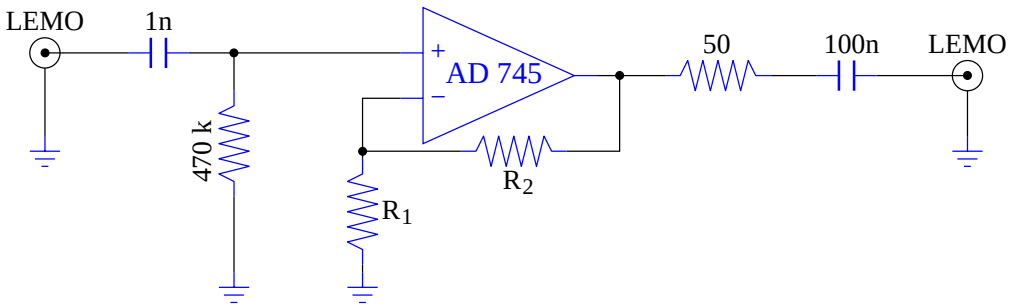


Figure 7.3: Schematic of the buffer amplifier.

There will be two readout methods used in energy and noise measurements. One method employs an external shaping amplifier for pulse shaping. The external shaping amplifier (Spectroscopy Amplifier from Canberra, model 1413, with adjustable gain and selectable shaping times of $1\mu s$, $2\mu s$, $4\mu s$, $8\mu s$ and $12\mu s$) is inserted between the buffer amplifier and MCA (see the block diagram in Figure 7.4a). The other method uses the shaper from the readout chip for pulse shaping (Figure 7.4b).

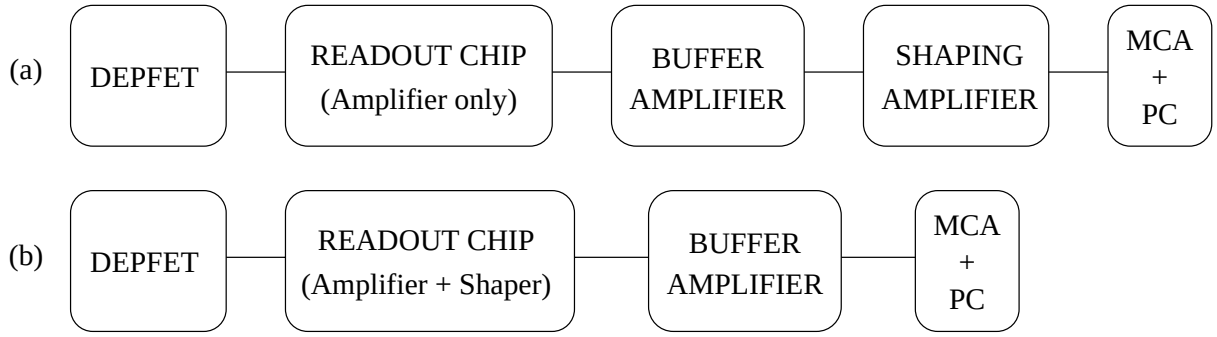


Figure 7.4: Readout schemes used in energy and noise measurements.

7.1.1 Multi-Channel Analyzer (MCA) calibration

The output voltage signal of the DEPFET readout system is digitized by an MCA PC-card, model MCDLAP from Fast ComTec[2]. The MCA card employs a 14 bit ADC (i.e. 16384 channels) with an input voltage range of 8V. The maximum input voltage resolution is 0.5mV.

The MCA card is calibrated with respect to the amplitude of the input voltage. The MCA input voltage is taken from a pulse generator in combination with a shaping amplifier (to generate semi-gaussian voltage pulses). Its amplitude is measured with the oscilloscope. Figure 7.5 shows the dependence between the amplitude of the input voltage pulse and the corresponding channel number of the MCA. The linear dependence is

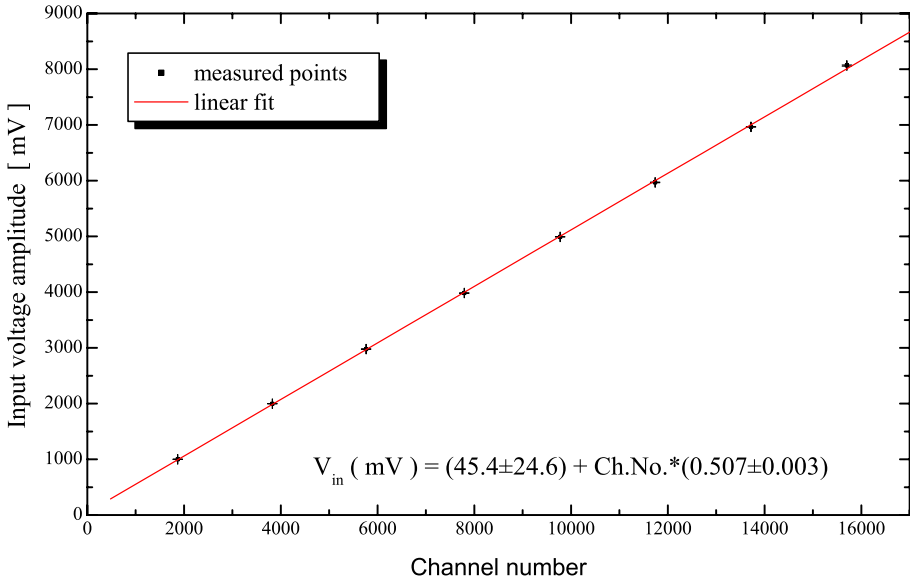


Figure 7.5: Calibration of the multi-channel analyzer.

obtained from the straight line fit.

[2]www.fastcomtec.com

7.2 Measurements with DEPFET Type-I and II

This section presents energy and noise measurements performed with DEPFET structures of Type-I and Type-II. Recalling the description of the DEPFET devices in section 2.5, the two DEPFET structures are identical except for the clear mechanism (punch-through structure for Type-I and MOSFET structure for Type-II).

The first investigations with the ^{55}Fe source revealed the range of the DEPFET parameters (bias voltages and currents) which insures a proper operation of the detector. The values of these parameters are listed in Table 7.2. It has been found that variations

Parameter	Description	Min. value	Max. value
V_{dr}	Drain voltage	-15 V	-3 V
V_{cl} (Type-I)	Clear voltage	5 V	6.5 V
V_{cl} (Type-II)	Clear voltage	10.5 V	12 V
V_{back}	Depletion voltage	-100 V	-60 V
V_{R3}	Voltage on the external guard ring	-50 V	-25 V
V_{R1}	Voltage on the internal guard ring	-25 V	-12 V
I_{ds}	JFET current	1 μA	100 μA

Table 7.2: Values of the DEPFET parameters

of some of these parameters have a significant influence on the detector noise performance. A detailed investigation of these influences is presented in the following sub-sections.

7.2.1 Influence of V_{dr} on the DEPFET performance

Measurements with the ^{55}Fe source have shown that the DEPFET signal gain increases with the absolute value of V_{dr}. Figure 7.6 shows the amplitude of the DEPFET output signal (i.e. voltage signal at DEPFET source) as a function of the drain voltage. The signal corresponds to the Mn-K$_\alpha$ energy peak of ^{55}Fe.

The variation of the signal gain can be explained by the change of the total capacitance at the internal gate (i.e. C_{gd} in expression 4.5 of the DEPFET signal gain) with the drain voltage. This capacitance has a component which can be seen as a depletion capacitance between gate and drain. As the depletion capacitance decreases with the depletion voltage, the total capacitance will decrease with the absolute value of V_{dr}.

Knowing that the electrical charge generated by the Mn-K$_\alpha$ photon in silicon is 0.259 fC, the total capacitance at the internal gate can be calculated using the approximation from equation 4.6. The total gate capacitance of the DEPFET Type-I varies between $53 \pm 5\ fF$ at $V_{dr} = -3V$ and $37 \pm 4\ fF$ at $V_{dr} = -15V$.

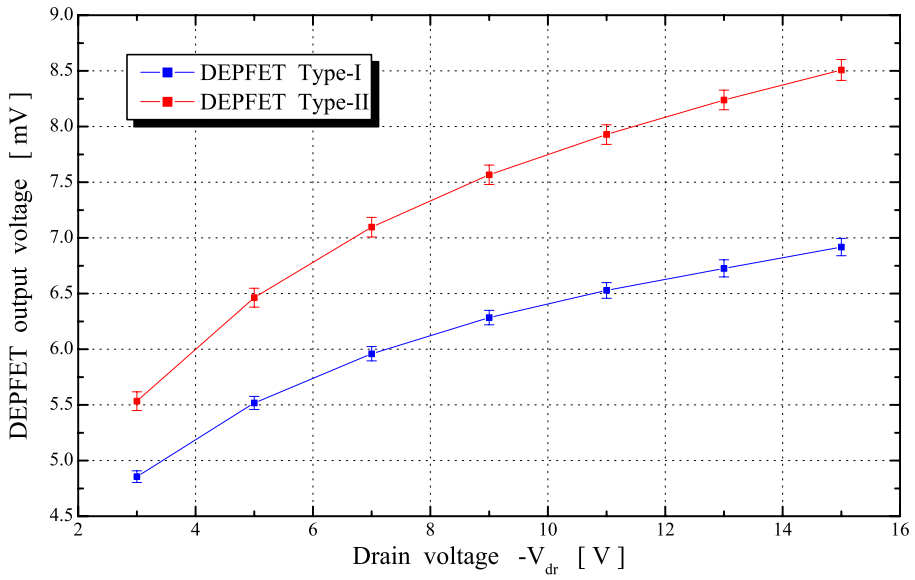


Figure 7.6: DEPFET output signal corresponding to Mn-K$_\alpha$ energy versus V_{dr}.

One can see in Figure 7.6 that the output signal measured for the DEPFET Type-II is about 20% larger than that of DEPFET Type-I, which means that the internal gate capacitance is correspondingly smaller.

The total noise of the DEPFET system depends also on the drain voltage. With the radioactive source away from the detector, the root mean square (rms) value of the output noise voltage is measured with the digital oscilloscope at the same values of the drain voltage. Knowing the amplitude of the output signal corresponding to Mn-K$_\alpha$ energy, the equivalent input noise charge (ENC) is easily calculated. Figure 7.7 shows the ENC noise values for both DEPFET types plotted as a function of the drain voltage. The noise curves have a minimum around $V_{dr} = -11V$. The ENC noise is lower for the DEPFET Type-II (the internal gate capacitance is smaller).

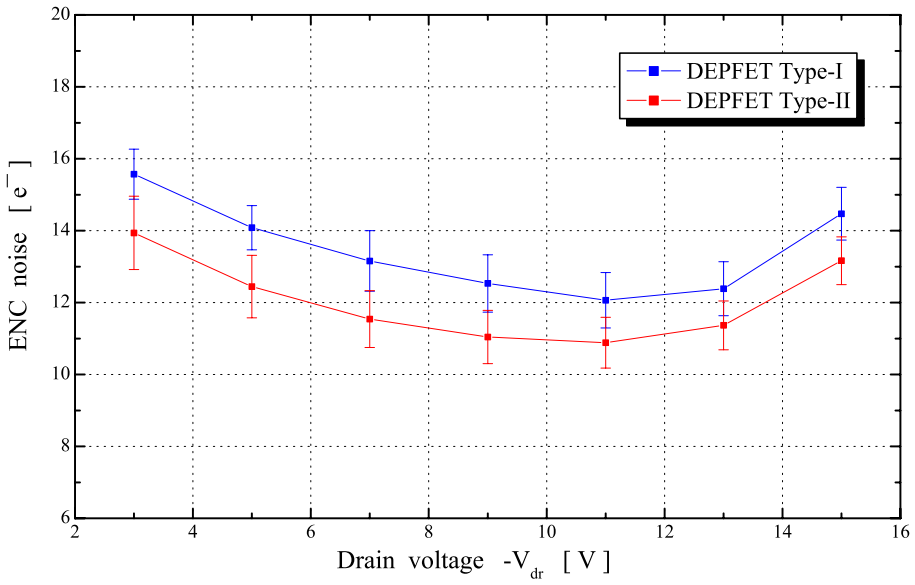


Figure 7.7: ENC noise versus drain voltage.

7.2.2 Influence of I_{ds} on the detector performance

With the drain voltage set to $V_{dr} = -8V$, the amplitude of the output signal of the Mn-K$_\alpha$ energy is measured at different values of the JFET current I_{ds}. Figure 7.8 shows the DEPFET output signal plotted as a function of I_{ds}. For current values higher than

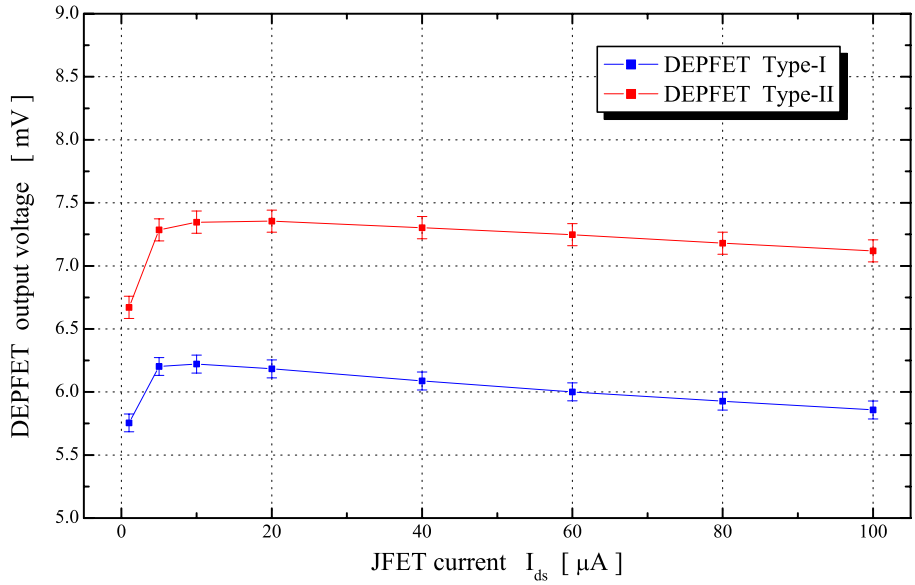


Figure 7.8: DEPFET output voltage from Mn-K$_\alpha$ energy versus I_{ds}.

$10\mu A$, the amplitude of the signal decreases with the increasing value of I_{ds} (g_{ds} in the DEPFET gain equation 4.5 increases with I_{ds}).

The input noise dependence on the JFET current is plotted in Figure 7.9 The noise

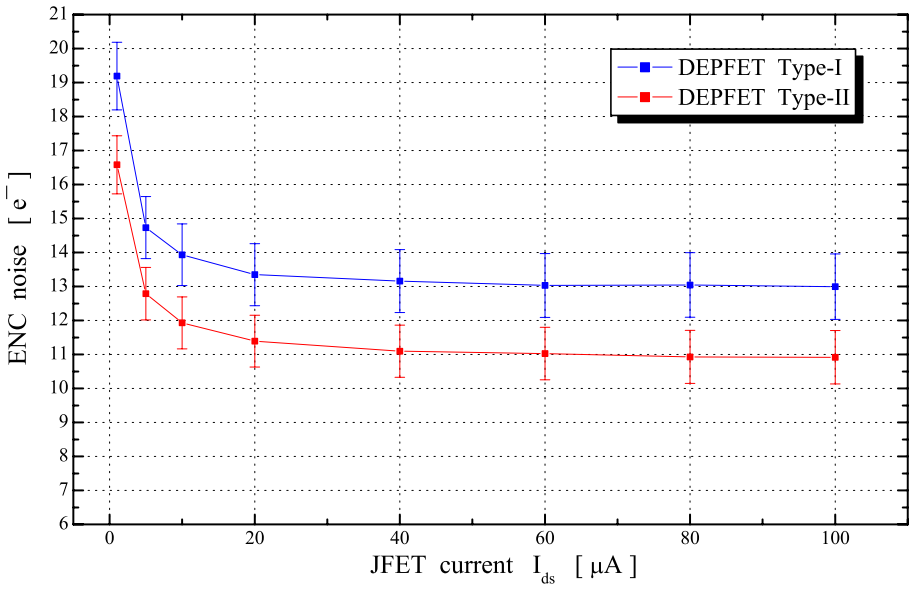


Figure 7.9: ENC noise versus I_{ds}.

increases at low values of I_{ds} and remains almost constant for current values higher than $20\mu A$.

7.2.3 Measurement of ENC noise versus shaping time

The noise dependence on the shaping time is investigated using the readout scheme in Figure 7.4a. The value of the shaping time τ is set in the external shaping amplifier. The DEPFET drain is biased at $V_{dr} = -10V$, the JFET current is $I_{ds} = 30\mu A$. Like in the previous measurements, the noise is measured with the oscilloscope as output voltage noise and referred to the input as ENC noise. The values of the ENC noise are plotted in Figure 7.10. For lower values of the shaping time the noise decreases with τ (thermal noise contribution). The noise curve reaches a minimum between 2 and 4 μs and increases then with the value of the shaping time (shot noise contribution). A function of the form:

$$ENC_{fit}(\tau) = \sqrt{a \cdot \tau + \frac{b}{\tau} + c} \tag{7.1}$$

is fitted to the data points. The final values of the fit parameters a, b and c are also shown in the graph. The minimum values of the ENC noise for both DEPFET types are:

$$\text{DEPFET Type-I:} \quad ENC_1^{min} = 12.4 \pm 0.6\, e^- \ \text{ at } \ \tau_{min} \approx 2.8\mu s$$
$$\text{DEPFET Type-II:} \quad ENC_2^{min} = 11.1 \pm 0.7\, e^- \ \text{ at } \ \tau_{min} \approx 2.2\mu s$$

From the values of the fit parameters in the function ENC_{fit} one can determine the individual contribution of each noise term (i.e. thermal noise, shot noise and flicker noise).

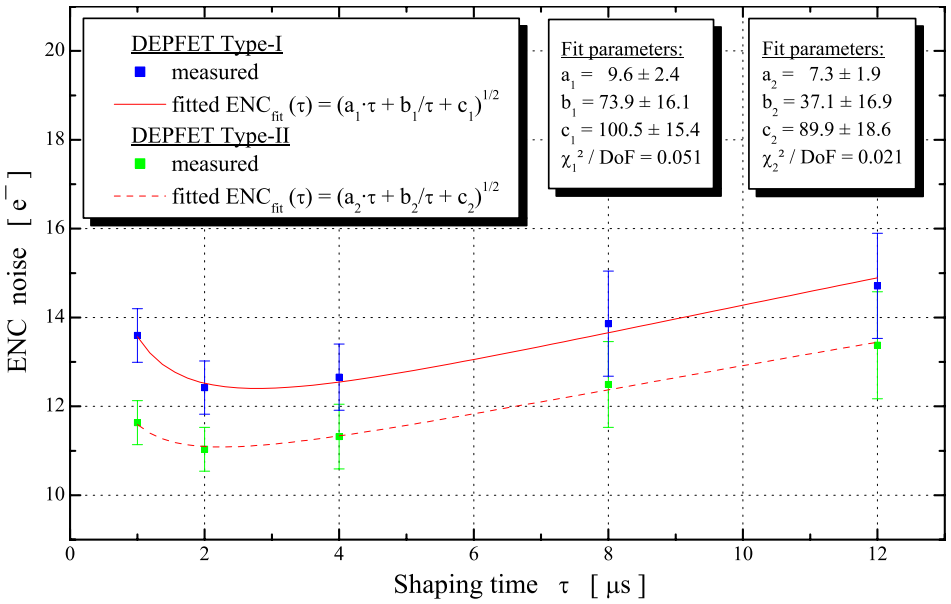


Figure 7.10: ENC noise versus shaping time.

The major contribution is given by the flicker noise term (parameter c in $ENC_{fit}(\tau)$) which represents about 65% of the total noise.

The noise contribution of the readout electronics (amplifier in the readout chip, buffer amplifier and shaper) measured by measuring the rms value the output noise with the DEPFET detector disconnected is:

$$ENC_{readout} = 5.3 \pm 0.5\, e^-$$

and represents about 20% of the total noise.

7.2.4 Measurements of the x-ray spectrum of ^{55}Fe radioactive source

The x-ray spectrum of the radioactive source ^{55}Fe is measured using both setups described in Figure 7.4. The first measurements are performed with the setup containing the external shaping amplifier (Figure 7.4a). The shaping time is set close to the minimum noise value, i.e $\tau = 2\mu s$. The energy spectrum measured with the DEPFET Type-I is plotted in Figure 7.11.

Apart from the two energy peaks corresponding to Mn-K$_\alpha$ and Mn-K$_\beta$ lines, one encounters a continuous background at lower energies. This background is produced by the so-called *split events*. A split event occurs when only a fraction of the total energy is deposited within the pixel area (which is about $120 \times 140 \mu m^2$). The split events cause also a broadening of the main energy peaks toward lower energy. To avoid this unwanted contribution when determining the energy resolution of the system, a gaussian function is fitted to the right side of the energy peak. The energy resolution (expressed in terms

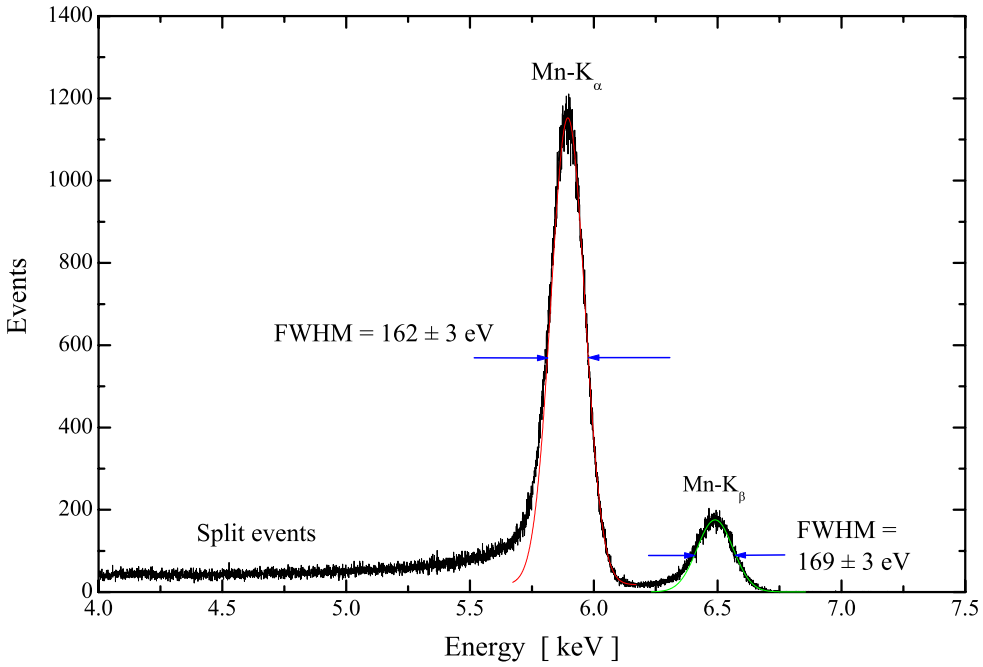


Figure 7.11: Energy spectrum of ^{55}Fe measured with DEPFET Type-I.

of FWHM[3]) obtained from the gauss fit is:

$$FWHM_{Mn-K_\alpha} = 162 \pm 3eV$$
$$FWHM_{Mn-K_\beta} = 169 \pm 3eV$$

The ENC noise value can be determined from the energy resolution using the formula:

$$ENC^2 = \left(\frac{FWHM}{2\sqrt{2 \cdot ln2} \cdot w}\right)^2 - \frac{F \cdot E}{w} \tag{7.2}$$

where w= 3.64 eV is the mean ionization energy in Si, E is the energy of the x-ray and F is Fano factor. The second term in the equation 7.2 is the noise due to the statistical spread of the ionization process inside the detector (i.e. Fano noise, see section 4.3.2 for details). For silicon detectors, $F = 0.123$ at 5.895 keV and $F = 0.126$ at 6.490 keV [Per99]. Replacing the values of the energy resolution (FWHM) into the equation 7.2, one obtains:

$$ENC \approx 12.6e^- \quad \text{for Mn-K}_\alpha$$
$$ENC \approx 12.8e^- \quad \text{for Mn-K}_\beta$$

which are consistent with the value determined in section 7.2.3.

The energy spectrum recorded in the same conditions with the DEPFET Type-II is plotted in Figure 7.12. The energy resolution values determined from the gauss fit of

[3]Full Width Half Maximum

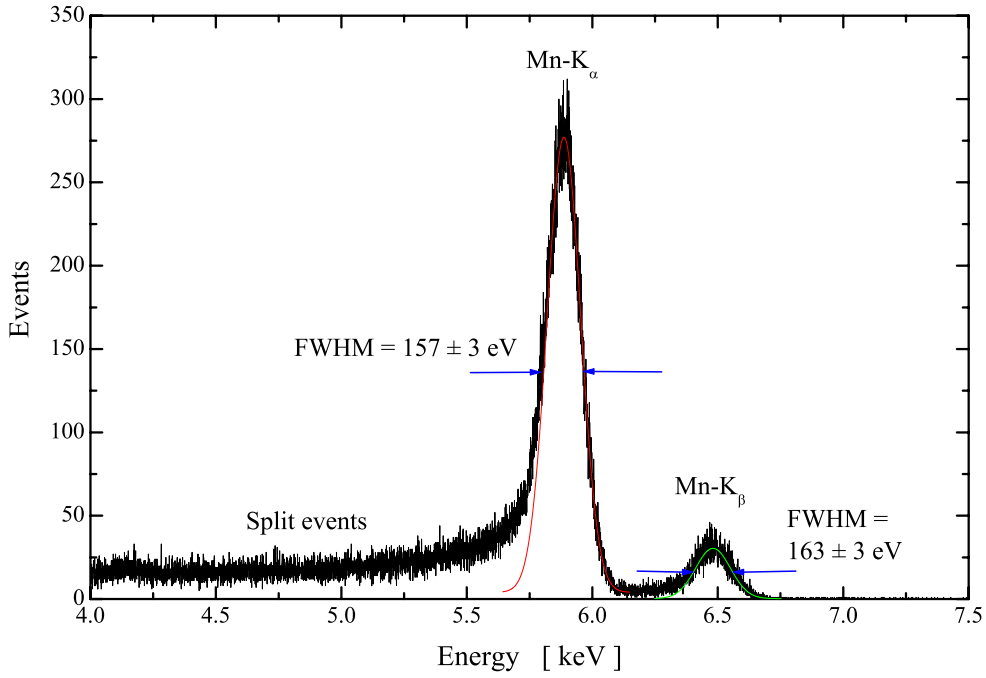


Figure 7.12: Energy spectrum of ^{55}Fe measured with DEPFET Type-II.

the two energy peaks are:

$$FWHM_{Mn-K_\alpha} = 157 \pm 3eV$$
$$FWHM_{Mn-K_\beta} = 163 \pm 3eV$$

and the corresponding values of the ENC noise are:

$$ENC \approx 11.7e^- \quad \text{for Mn-K}_\alpha$$
$$ENC \approx 11.6e^- \quad \text{for Mn-K}_\beta$$

Comparing with the values determined for the DEPFET Type-I, one can see again that the DEPFET device of Type-II has lower noise contribution due to its smaller input capacitance at the internal gate.

The energy spectrum from ^{55}Fe is measured now using the setup described in Figure 7.4b. The pulse shaping is performed with CRRC shaper from the readout chip (see section 5.5.2). The time constant of the shaper is $\tau \approx 1.8\mu s$, the drain voltage is $V_{dr} = -10V$ and the JFET current is $I_{ds} = 30\mu A$. The energy spectrum measured with the DEPFET Type-I is plotted in Figure 7.13. The values of the energy resolution at Mn-K$_\alpha$ and Mn-K$_\beta$ are:

$$FWHM_{Mn-K_\alpha} = 173 \pm 3eV$$
$$FWHM_{Mn-K_\beta} = 179 \pm 3eV$$

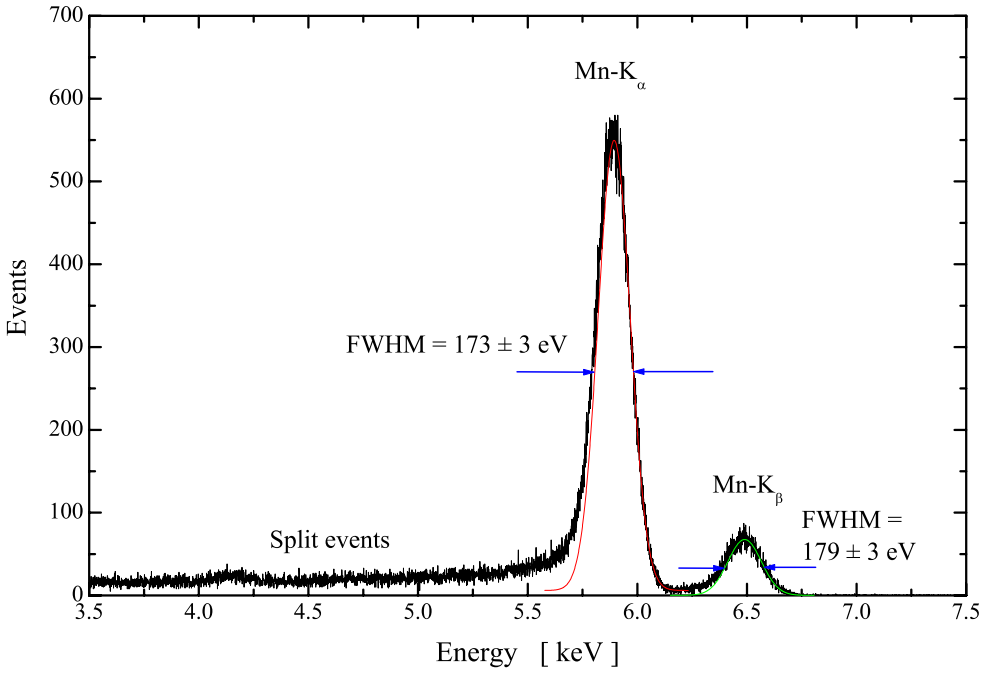


Figure 7.13: Energy spectrum of ^{55}Fe measured with DEPFET Type-I.

Replacing the FWHM values in the formula of equation 7.2, the following values of the ENC noise are obtained:

$$ENC \approx 14.5e^- \quad \text{for Mn-K}_\alpha$$
$$ENC \approx 14.6e^- \quad \text{for Mn-K}_\beta$$

The noise values are larger than in the previous measurements due to the noise contribution of the CRRC shaper from the readout chip.

The spectrum measured in the same conditions with the DEPFET Type-II is shown in Figure 7.14. The ENC noise values obtained from the energy resolution are:

$$ENC \approx 12.9e^- \quad \text{for Mn-K}_\alpha$$
$$ENC \approx 12.8e^- \quad \text{for Mn-K}_\beta$$

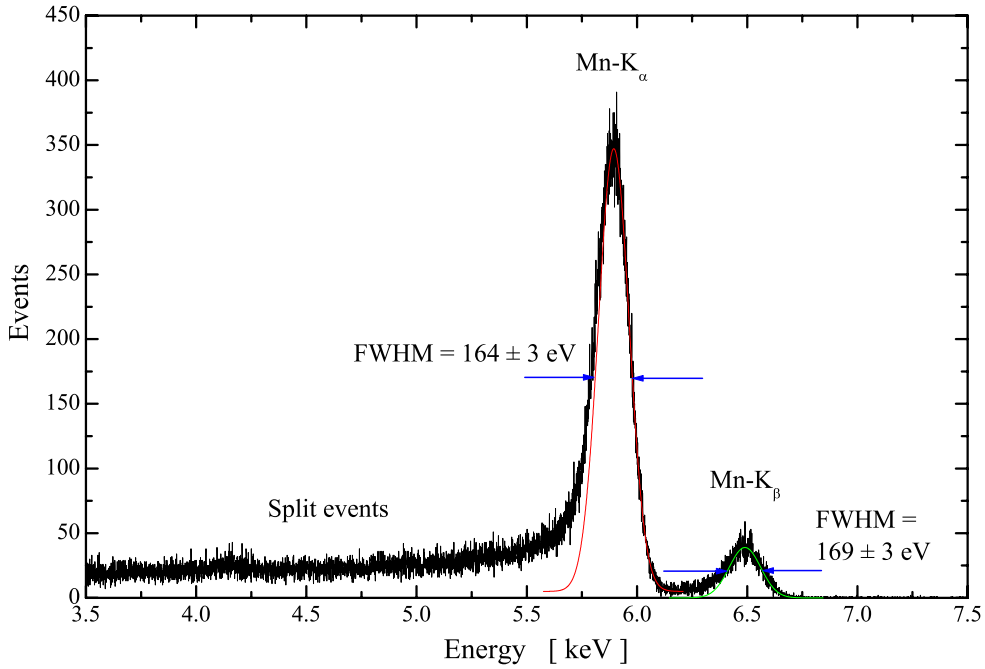


Figure 7.14: Energy spectrum of ^{55}Fe measured with DEPFET Type-II.

7.2.5 Measurement of the x-ray spectrum of ^{109}Cd radioactive source

The energy spectrum of the radioactive source ^{109}Cd measured with the DEPFET Type-I is plotted in Figure 7.15.

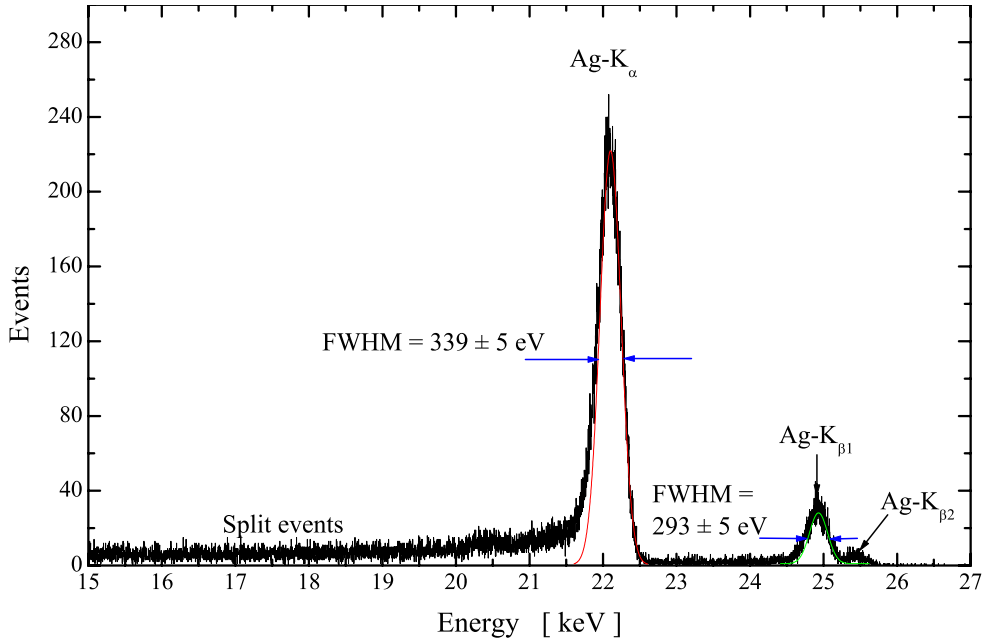


Figure 7.15: Energy spectrum of ^{109}Cd with DEPFET Type-I.

Apart from the Fano broadening, the energy peak Ag-K_α has also an intrinsic broadening caused by the fact that there are two separate transitions energies (Ag-$K_{\alpha 2}$ at 21.99 keV and Ag-$K_{\alpha 1}$ at 22.16 keV) which contributes to the energy peak. The corresponding FWHM value is therefore larger.

7.3 Measurements with DEPFET Type-III and IV

Similar energy measurements with DEPFET devices of Type-III and IV (different JFET transistor) were not possible due to the fact that the JFET transistor on the structures without external gate contact does not work properly. Figure 7.16 shows the static characteristics of the JFET transistor of a DEPFET of Type-III from the structure with and without external gate contact. The characteristics are measured with the detector

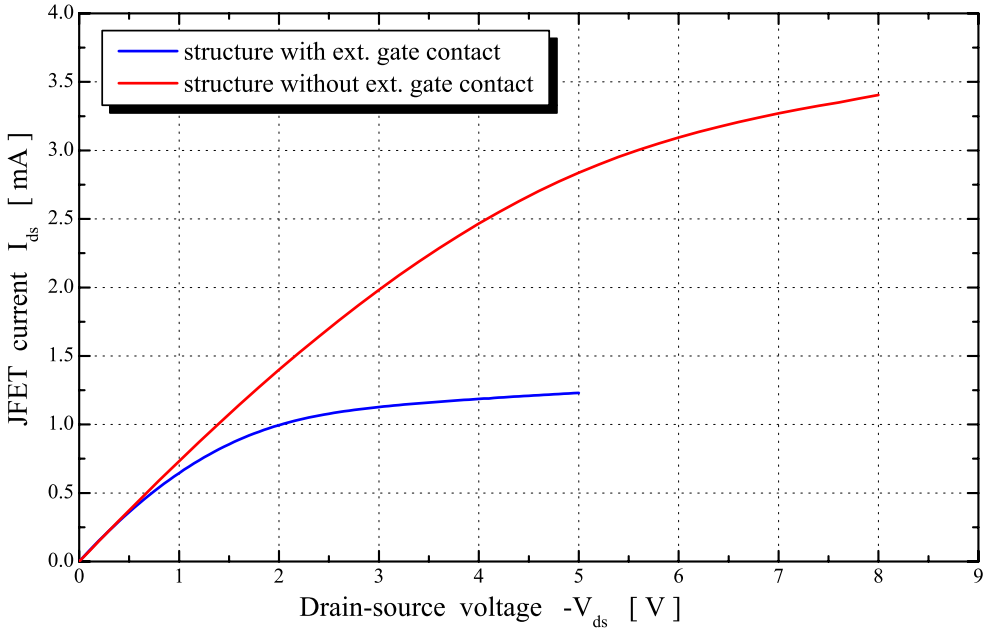


Figure 7.16: JFET characteristics of a DEPFET Type-III with and without external gate contact.

substrate connected to ground (i.e. the gate potential is zero).

One can see that characteristic of the JFET without external gate contact differs significantly from the characteristic of the other JFET, especially at large values of the drain-source voltage. The saturation region is not well defined showing that the JFET channel does not really reach the pinch-off point. This conclusion was confirmed also by the measurements with the detector substrate depleted. Increasing the clear voltage, the JFET current decreases at much slower rate than in the JFET with external gate contact and never reaches the null value (compare with measurements in Figure 3.10). With $V_{dr} = -5V$, the minimum current value of about $350\mu A$ is reached at a maximum clear voltage $V_{cl} \approx 25V$. This large current value can not be supplied by the current source in the readout chip.

The reason for this anomalous behaviour can be found in the implantation profile of the external gate. When the external gate is provided with a contact, a heavily doped n^+ implant is added to the external gate implant (also of type n) in order to form a good ohmic contact with the metal layer of the external contact. When the external gate contact misses, this heavily doped implant also misses. The doping concentration of the gate implant is not high enough to deplete the whole JFET channel and the transistor can not reach the pinch off region.

Chapter 8

Summary and outlook

A short summary of the thesis work as well as an overview on possible applications of DEPFET pixel detectors are given in this chapter.

8.1 Summary and conclusions

DEPFET detector structures with continuous clear mechanism have been investigated within the framework of this thesis. The DEPFET pixel detector is a detector structure with integrated amplifying mechanism (also called active pixel sensor). The generated signal charge is collected at the internal gate of a JFET transistor integrated directly on the detector substrate. The transistor represents the first amplifying stage of the detector readout circuit. Beside the advantage of the internal amplification of the signal charge, the detector exhibits a very small input capacitance (tens of fF) which insures a very low noise and hence, an outstanding energy resolution capability even at room temperature.

Single DEPFET pixel structures with different types of clear mechanism (punch-through structure or MOSFET structure) and different types of JFET transistors have been characterized and their static characteristics have been measured.

A theoretical analysis of the DEPFET noise performance has been carried out. Based on these calculations, a low-noise analog readout has been designed as a dedicated ASIC using the planar CMOS technology (AMS-0.6μm process). The readout consists of a feedback voltage amplifier followed by a semi-gaussian shaper and an output buffer. A current source for biasing the JFET transistor on the DEPFET is also integrated in the readout. The readout is foreseen to be implemented later on in a readout matrix for 32×32 DEPFET matrix structure.

The two different DEPFET structures which were used in energy measurements have identical JFET transistors, but different clear mechanisms. By evaluating the energy spectrum of ^{55}Fe, an electronic noise of about $13e^-$ was measured at room temperature.

Further improvements in the analog readout can be achieved by increasing the voltage gain of the feedback amplifier. Having measured the value of the DEPFET signal gain ($\approx 1mV/keV$), the gain of the feedback amplifier can be increased up to 50 for an input energy range up to 30 keV. This will reduce the noise contribution of the shaper to about 10% of the total noise. The semi-gaussian shaper should be designed also with an intrinsic gain (G_{sh} in equation 5.60) larger than 1. To obtain an amplitude ratio of 1:1 between

output and input signals of the shaper, the shaper signal gain G_{sh} should be made equal to e.

Integrated into a readout matrix for a matrix of DEPFET pixels, the readout system could be made self-triggering. Such a system is under investigation [Haus02].

8.2 Possible applications of DEPFET pixel detectors

The DEPFET pixel detector can find its use in a large variety of application fields such as medicine, biology, astronomy or experimental particle physics. Some of the projects which can benefit from the high energy resolution capabilities of the DEPFET detector will be presented here.

Compton camera for medicine

The Compton camera [Bla98, Kuy88] is an attractive alternative to the classical methods used in medicine for imaging parts of the human body. In contrast to the up-to-date imaging methods, i.e. SPECT[1] or PET[2] which make use of mechanical collimators, the Compton camera utilizes the kinematics of the Compton scattering to localize the original direction of the γ-ray emitted from a source distribution. The working principle of the Compton camera is explained in Figure 8.1. The system consists basically of two detector

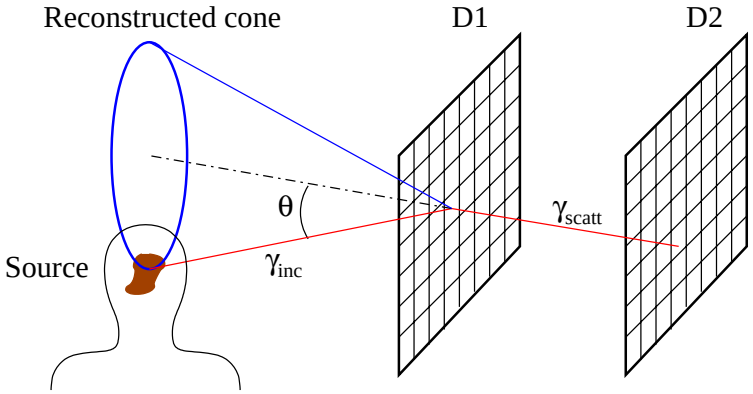


Figure 8.1: Working principle of a Compton camera.

layers D_1 and D_2. Compton scattering takes place at D_1, while the scattered photon is absorbed by photoelectric effect in the detector D_2. Both detector layers are pixelized, making possible to determine the positions of the Compton scattering and the absorption points. Additional, the energy of the recoil electron is measured in the scattering detector D_1. With the energy of the recoil electron and the position and the direction of the scattered photon determined, the scattering angle θ can be calculated (see the kinematics of the Compton scattering in section 1.1.2). A reconstructed cone at the angle θ with respect to the central axis (the direction of the scattered photon) intersects the source of

[1] Single Photon Emission Computed Tomography
[2] Positron Emission Tomography

the incident γ-ray. The intersection of individual cones from the same point source will give the three dimensional position of the source. The main advantage of the Compton camera over SPECT and PET detectors is that it could deliver images of similar qualities at much lower radiation doses.

The finite energy resolution of the recoil electron translates into an uncertainty for the scattering angle which in turn affects the quality of the reconstructed image. With its high energy resolution capability and its high pixelisation potential, the DEPFET pixel detector is a good candidate for the scattering detector of the Compton camera.

Digital autoradiography

Autoradiography is a widely used method in biomedical sciences for determining the distribution of a radioactive material (called *tracer*) within biological tissues. A tissue probe is injected with a radioactive substance and then placed on a detector (photographic film, solid state detector). An image showing the two dimensional distribution of the intensity of the radioactive material gives information about the structure of the probe.

The predominant medium for autoradiography at present is still photographic film. Beside the advantages of low cost and excellent spatial resolution ($< 1\mu m$), the film has however a few important drawbacks: long exposure and developing time, no energy resolution, limited dynamic range, non-linear response function. These disadvantages are overcome in the digital radiography [Ove98] by using new types of detectors such as multi-wire proportional counters, scintillator based detectors, micro-strips detectors, CCDs or pixel sensors. The state-of-the-art silicon pixel detectors combine the advantages of high energy resolution, good spatial resolution, high dynamic range and good linearity. A bioscope system based on a DEPFET pixel matrix was already successfully used at Bonn University [Nees00, Ulr03], for the detection of tritium (^{3}H) which is one of the radio-labels commonly used in autoradiography.

X-ray astronomy

DEPFET pixel detectors can find their application in x-ray astronomy as well. With their low noise figures, they are appropriate detector devices for soft and medium energy x-rays which are of interest for the x-ray satellite missions. After the successful launch of the X-ray Multi Mirror (XMM) satellite mission [XMM03] in 2000, equipped with a $6 \times 6cm^2$ pn-CCD detector [Str00] ($150 \times 150\mu m$ pixel size), a new satellite mission named XEUS (X-ray Evolving Universe Spectroscopy) [XEUS03] will follow in 2010.

XEUS is an x-ray space telescope [Str00] which will be used to measure x-ray objects situated at huge distances in the universe and to find out information about their origin. A picture of the telescope is shown in Figure 8.2. The telescope consists of two separate modules: the mirror spacecraft (MSC) containing x-ray mirror plates and the detector spacecraft (DSC) situated in the focal plane of the mirror and containing the detector modules. The distance between the two modules (i.e. focal length of the x-ray mirror) is 50m. The relative position of the detector with respect to the mirror will be maintained with an accuracy of $\pm 1mm^3$. After 4-6 years after the launch, the XEUS mission will take advantage of the presence of the International Space Station (ISS) to refurbish and upgrade its modules.

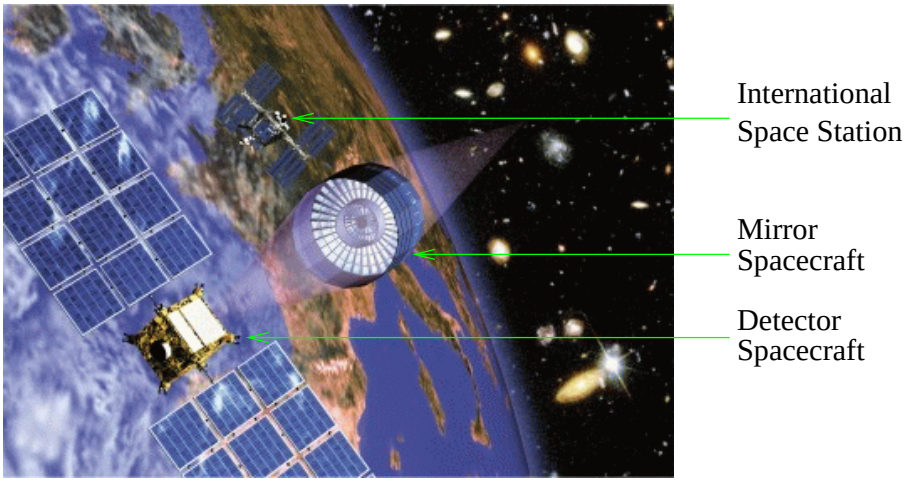


Figure 8.2: Picture of the XEUS space telescope with the International Space Station (ISS) [ESA00].

The XEUS telescope is planned to a have a collecting area 20 times larger than XMM, which requires larger area detectors with higher counting capability. Thus, new detector concepts must replace the rather slow pn-CCD detectors used in XMM.

A DEPFET matrix of 1024×1024 pixels ($75 \times 75 \mu m^2$ pixel size) is proposed as the detector for the XEUS telescope. This will allow the measurement of the position, arrival time and energy with sufficiently high accuracy in the energy range from 0.1 to 30 keV [Str00].

Experimental particle physics

Experimental particle physics has always been a driving force behind the development of more sophisticated detectors. With the new generation of accelerators where the impact energy is pushed higher and higher, the demand on larger area detectors capable of coping with very high counting rates has become obvious. Silicon pixel detectors are very attractive as vertex detectors for high energy applications due to their performances regarding both the position and energy resolution. DEPFET pixel detectors are a viable alternative to the classical silicon detectors in applications where the requirements on energy resolution are very strict. As an example, the vertex detector of the linear accelerator TESLA [TDR01] is planned to be equipped with DEPFET pixel layers. More details in this subject can be found in [Koh03].

Appendix A

Frequency analysis of the regulated cascode amplifier

A detailed treatment of the high frequency analysis of the regulated cascode amplifier will be presented in this appendix. An appropriate method of frequency compensation of the circuit is described at the end.

A.1 Stability problem in feedback amplifiers

Consider the general structure of a feedback amplifier system sketched in Figure A.1. $A(s)$ and $\beta(s)$ are the frequency dependent[1] transfer functions of the amplifier and feed-

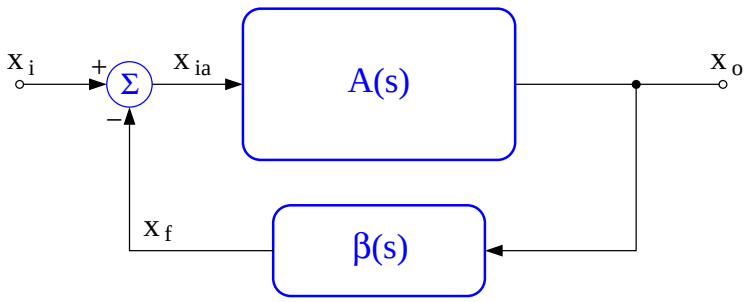


Figure A.1: Block diagram of a general feedback amplifier.

back loop, respectively. The feedback signal $x_f = \beta x_o$ is subtracted[2] from input signal x_i to produce the signal x_{ia} which is the input to the basic amplifier. It follows that the closed-loop transfer function is given by:

$$A_{fb}(s) = \frac{x_o}{x_i} = \frac{A(s)}{1 + \beta(s)A(s)} \tag{A.1}$$

[1]Note that $s = j\omega = j2\pi f$, where f is the frequency.
[2]The subtraction or the addition of x_f determines whether the feedback is negative or positive.

The loop gain $A(s)\beta(s)$ is a complex number which can be represented by its magnitude and phase:

$$A(s)\beta(s) = |A(j\omega)\beta(j\omega)|e^{j\Phi(j\omega)} \tag{A.2}$$

The manner in which the loop gain varies with frequency determines the stability or instability of the feedback amplifier.

Consider the frequency denoted by ω_{180^o} at which the phase of the loop gain becomes 180^o. If the magnitude of the loop gain at this frequency is equal to 1, it follows from equation A.1 that $A_{fb}(j\omega_{180^o})$ will be infinite and sustained oscillations will occur. To prevent that, the condition:

$$|A(j\omega_{180^o})\beta(j\omega_{180^o})| < 1 \tag{A.3}$$

must be fulfilled. Another convenient way to express this requirement is $\Phi(\omega_{0\ \mathrm{dB}}) < 180^o$, where $\omega_{0\ \mathrm{dB}}$ is the frequency corresponding to the unity magnitude of the loop gain.

A measure of the stability of the system is given by the so-called *phase margin*. This is defined as the difference between the phase angle at $\omega_{0\ \mathrm{dB}}$ and 180^o. Figure A.2 shows the time response of a second-order closed-loop system [Alle02] with various phase margins. It can be seen that the larger values of the phase margin result in less "ringing" of the

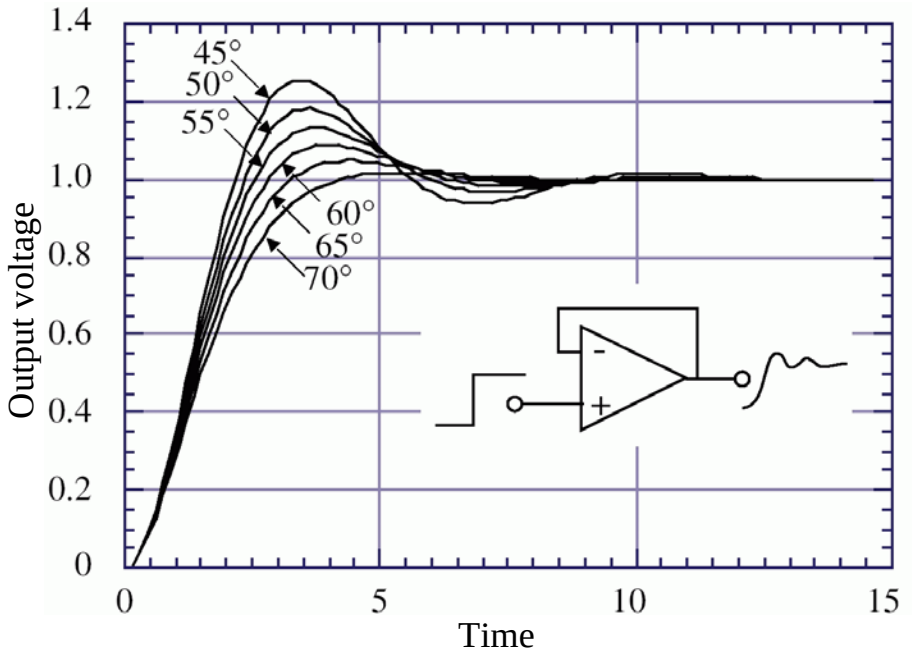


Figure A.2: Time response of a second order system with various phase margins [Alle02].

output signal. Phase margin values of at least 45^o (typically 60^o) are desirable in a feedback amplifier design.

As a conclusion of this discussion, the analysis of the stability of a feedback amplifier reduces to the frequency analysis of the amplifier loop gain $A(s)\beta(s)$. Assuming that $\beta(s)$ is a real and constant quantity as it is the case in most of the applications, this reduces to the analysis of the frequency dependence of the amplifier transfer function $A(s)$.

A.1.1 Frequency analysis: poles and zeros of $A(s)$

The function $A(s)$ which characterizes the frequency response of an amplifier takes the general form:

$$A(s) = \frac{a_o + a_1 s + ... + a_m s^m}{b_o + b_1 s + ... + b_n s^n} \tag{A.4}$$

where the coefficients a_i and b_i are real and $m \leq n$. It is a common practice to express $A(s)$ is terms of *poles* (defined as the roots of the denominator polynomial) and *zeros* (defined as the roots of the numerator polynomial. Since a_i and b_i are real numbers, the poles and zeros can be either real numbers or complex conjugate pairs. It is the location of the poles and zeros in the complex plane which gives the information about the frequency response and hence, about the stability of the system.

Consider now the case of a second order transfer function which is found in the analysis of many practical systems. For simplicity of the analysis, we assume that the function has only poles, i.e the numerator is a constant. The expression of the transfer function is therefore:

$$A(s) = \frac{A_o}{1 + \frac{2\xi}{\omega_o} s + \frac{s^2}{\omega_o^2}} \tag{A.5}$$

where $A_o = A(0)$ is the low-frequency gain, ω_o is called the pole frequency and ξ is called damping factor.

The two roots of the second order polynomial in the denominator are given by:

$$p_{1,2} = \begin{cases} -\omega_o \xi \pm j\omega_o \sqrt{1-\xi^2} & \text{if } 0 < \xi < 1, \\ -\omega_o \xi \pm \omega_o \sqrt{\xi^2 - 1} & \text{if } \xi \geq 1 \end{cases} \tag{A.6}$$

Figure A.3 shows the poles location in the complex plane and their movement with increasing values of ξ. For $0 < \xi < 1$ the complex conjugate poles move on a circle of

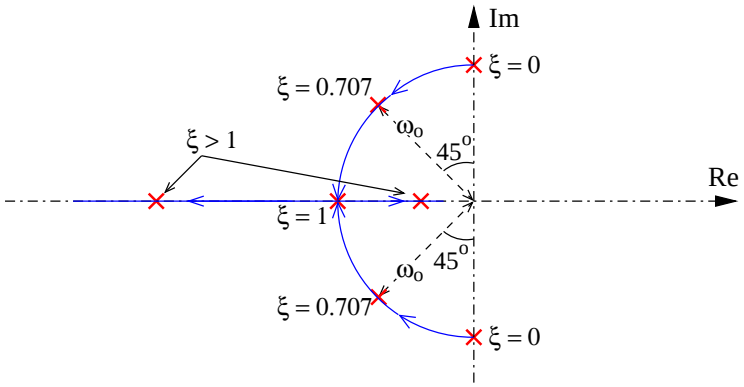


Figure A.3: Location of the poles in the complex plane for various values of ξ.

radius ω_o toward the real axis, as ξ approaches the unity. For $\xi^2 \gg 1$ their position on the negative real axis is given by:

$$p_1 \approx -2\xi\omega_o; \qquad p_2 \approx \frac{\omega_o}{2\xi} \tag{A.7}$$

One can remark that the case $\xi \leq 0$ is not considered here. The poles are in this case located in the right half of the complex plane. It can be shown [Sed98] that poles situated on the imaginary axis or in the right half of the complex plane give rise to instabilities, i.e. sustained or growing oscillations.

The magnitude and phase of the frequency dependent transfer function can be found from equation A.3 as:

$$\begin{aligned} |A(j\omega)| &= \frac{A_o}{\sqrt{\left(1-\frac{\omega^2}{\omega_o^2}\right)^2 + 4\xi^2\frac{\omega^2}{\omega_o^2}}} \\ \Phi(\omega) &= -\arctan\left[\frac{2\xi\frac{\omega}{\omega_o}}{1-\frac{\omega^2}{\omega_o^2}}\right] \end{aligned} \tag{A.8}$$

A plot of the two quantities versus radial frequency ω for $\omega_o = 10^6 rad \cdot Hz$ and various values of ξ is shown in Figure A.4. It can be seen that at low values of ξ the magnitude

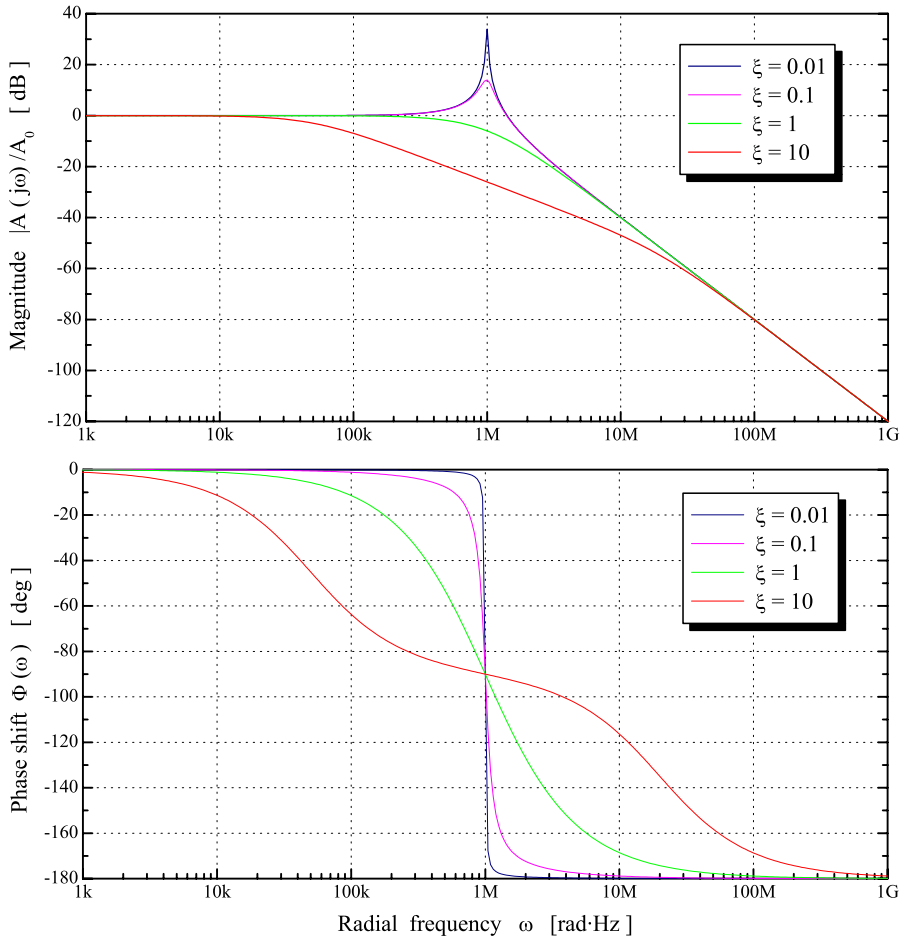


Figure A.4: Magnitude and phase of a second order transfer function

of the transfer function has a peak around ω_o (one can show that the peak occurs for

$\xi < \frac{1}{\sqrt{2}}$). Note that the presence of the peak is directly related to the occurance of the damped oscillations (see Figure A.2) in the time response of the system. The phase undergoes a step-like change of -180^o at ω_o.

A well defined split between the two poles occurs at larger values of ξ. Each pole introduces a phase shift of -90^o, while lowering the magnitude of $A(s)$ with 20 dB/decade.

Zeros in the amplifier transfer function can be analyzed in a similar way. Their effect is opposite to that of the poles. Thus, a real negative zero in the transfer function increases its magnitude with 20 dB/decade and introduces a phase shift of + 90^o. Care must be taken when a zero is situated in a right half of the complex plane. In terms of phase shift it acts like a negative pole, i.e introduces a phase shift of -90^o and could therefore degrade the phase margin of the system.

A.2 High frequency analysis of the RGC amplifier

The schematics of the RGC amplifier and its equivalent circuit for high frequency analysis are drawn in Figure A.5. The capacitances C_{gs2} and C_{gd3} connected in parallel have been

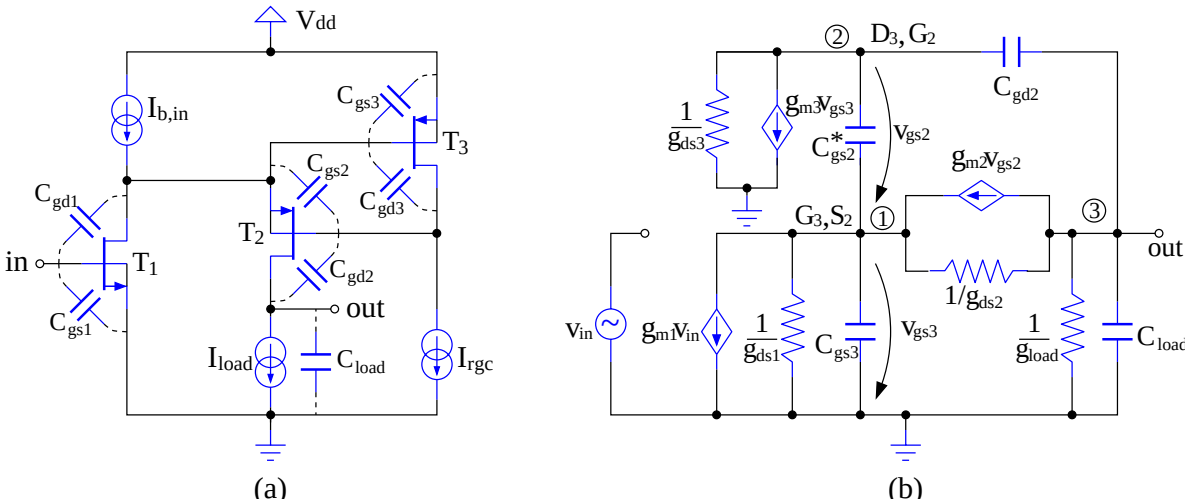


Figure A.5: (a) Schematic of the RGC amplifier and (b) its small signal equivalent circuit for high frequency analysis.

replaced by the equivalent capacitance C^*_{gs2}. Note that the implication of the capacitances C_{gs1} and C_{gd2} in the equivalent circuit is neglected. The former is just an input capacitance and acts as a load capacitance for the preceding stage, whereas the latter can be replace by an equivalent input capacitance by applying Miller's theorem [Sed98]. Moreover, it can be shown [Alle02] that C_{gd1} determines the occurance of a positive zero in the transfer function at the radial frequency $\frac{g_{m1}}{C_{gd1}}$. With g_{m1} very large (e.g. $\approx 700\mu S$ in the present design) and C_{gd1} of the order of fF (e.g. $\approx 20fF$), the zero occurs at frequencies beyond 10 GHz, and does not harm the transfer function characteristics.

The frequency dependent transfer function is found by applying Kirchoff's theorem for currents in the three nodes of the circuit in Figure A.5b:

$$\begin{aligned}
&① \quad {}_{m1}v_{in} + v_{gs3}(g_{ds1} + sC_{gs3}) - v_{gs2}sC^*_{gs2} - g_{m2}v_{gs2} + (v_{gs3} - v_o)g_{ds2} = 0 \quad : g\\
&② \quad {}_{gs2} + v_{gs3})g_{ds3} + g_{m3}v_{gs3} + v_{gs2}\cdot sC^*_{gs2} + (v_{gs2} + v_{gs3} - v_o)\cdot sC_{gd2} = 0 \quad : (A.9)\\
&③ \quad {}_o(g_{load} + sC_{load}) + (v_o - v_{gs2} - v_{gs3})sC_{gd2} + g_{m2}v_{gs2} + (v_o - v_{gs3})g_{ds2} = 0 \quad : v
\end{aligned}$$

Rearranging the terms in the equations above, one obtains:

$$\begin{aligned}
&② \quad {}_o sC_{gd2} + v_{gs2}\left[g_{ds3} + s\left(C^*_{gs2} + C_{gd2}\right)\right] + v_{gs3}(g_{m3} + g_{ds3} + sC_{gd2}) = 0 \quad : -v\\
&③ \quad {}_o\left[g_{load} + g_{ds2} + s\left(C_{load} + C_{gd2}\right)\right] + v_{gs2}(g_{m2} - sC_{gd2}) - v_{gs3}(g_{ds2} + sC_{gd2}) =: 0v\\
&① \quad {}_o\left[g_{load} + s\left(C_{load} + C_{gd2}\right)\right] - v_{gs2}s\left(C^*_{gs2} + C_{gd2}\right) + v_{gs3}\left[g_{ds1} + s\left(C_{gs3} - C_{gd2}\right)\right] =\\
&\quad = -g_{m1}v_{in}
\end{aligned} \quad (A.10)$$

The equation system A.10 can be written in a matrix form:

$$\widehat{\mathbf{M}}\cdot\begin{pmatrix} \frac{v_o}{v_{in}} \\ \frac{v_{gs2}}{v_{in}} \\ \frac{v_{gs3}}{v_{in}} \end{pmatrix} = -g_{m1}\cdot\begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix} \quad (A.11)$$

where matrix $\widehat{\mathbf{M}}$ is given by:

$$\widehat{\mathbf{M}} = \begin{pmatrix} -sC_{gd2} & g_{ds3} + sC_{gg2} & g_{ds3} + g_{m3} + sC_{gd2} \\ g_{load} + g_{ds2} + sC^*_{load} & g_{m2} - sC_{gd2} & -(g_{ds2} + sC_{gd2}) \\ g_{load} + sC^*_{load} & -sC_{gg2} & g_{ds1} + s(C_{gs3} - C_{gd2}) \end{pmatrix} \quad (A.12)$$

with $C^*_{load} = C_{load} + C_{gd2}$ and $C_{gg2} = C^*_{gs2} + C_{gd2}$.

The voltage transfer function of the amplifier is found from equation A.11 as:

$$\boxed{A_v(s) = \frac{v_o}{v_{in}} = -g_{m1}\cdot\frac{det(\widehat{\mathbf{M}'})}{det(\widehat{\mathbf{M}})}} \quad (A.13)$$

where

$$\widehat{\mathbf{M}'} = \begin{pmatrix} 0 & g_{ds3} + sC_{gg2} & g_{ds3} + g_{m3} + sC_{gd2} \\ 0 & g_{m2} - sC_{gd2} & -(g_{ds2} + sC_{gd2}) \\ 1 & -sC_{gg2} & g_{ds1} + s(C_{gs3} - C_{gd2}) \end{pmatrix} \quad (A.14)$$

One can see that $A(s)$ is a third order transfer function with two zeros and three poles. Their values will be determined in the following sub-sections.

A.2.1 Zeros of the transfer function

The zeros of the voltage transfer function from equation A.13 are given by the roots of:

$$det(\widehat{\mathbf{M}'}) = det\begin{pmatrix} g_{ds3} + sC_{gg2} & g_{ds3} + g_{m3} + sC_{gd2} \\ g_{m2} - sC_{gd2} & -(g_{ds2} + sC_{gd2}) \end{pmatrix} \tag{A.15}$$

After grouping the coefficients of s^0, s^1 and s^2 the above expression becomes:

$$det(\widehat{\mathbf{M}'}) = -g_{ds2}g_{ds3}\left\{1 + a_{o2}(a_{o3}+1) + s\left[\frac{C_{gg2}}{g_{ds3}} + \frac{(g_{m2}-g_{m3})C_{gd2}}{g_{ds2}g_{ds3}}\right] + s^2\frac{C^*_{gs2}C_{gd2}}{g_{ds2}g_{ds3}}\right\} \tag{A.16}$$

where

$$a_{o2} = \frac{g_{m2}}{g_{ds2}}; \quad a_{o3} = \frac{g_{m3}}{g_{ds3}} \tag{A.17}$$

are the intrinsic gain expression of the transistors T_2 and T_3, respectively. Since $a_{o2}, a_{o3} \gg 1$, equation A.16 becomes:

$$det(\widehat{\mathbf{M}'}) = -g_{m2}g_{m3}\left\{1 + s\left[\frac{C_{gg2}}{g_{m3}a_{o2}} + \frac{(g_{m2}-g_{m3})C_{gd2}}{g_{m2}g_{m3}}\right] + s^2\frac{C^*_{gs2}C_{gd2}}{g_{m2}g_{m3}}\right\} \tag{A.18}$$

Using again the approximation $a_{o2} \gg 1$, the first term in the coefficient of s can be neglected. The equation for zeros reduces to:

$$1 + s\frac{(g_{m2}-g_{m3})C_{gd2}}{g_{m2}g_{m3}} + s^2\frac{C^*_{gs2}C_{gd2}}{g_{m2}g_{m3}} = 0 \tag{A.19}$$

with the solutions

$$\boxed{z_{1,2} = -\omega_{oz}\xi_z \pm \omega_o\sqrt{\xi_z^2 - 1}} \tag{A.20}$$

where

$$\begin{aligned} \omega_{oz}^2 &= \frac{g_{m2}g_{m3}}{C_{gd2}C^*_{gs2}} \\ \xi_z &= \frac{g_{m2}-g_{m3}}{2\sqrt{g_{m2}g_{m3}}}\sqrt{\frac{C_{gd2}}{C_{gs2}}} \end{aligned} \tag{A.21}$$

A.2.2 Poles of the transfer function

The poles in the voltage transfer function $A_v(s)$ are obtained as the roots of the denominator $det(\widehat{\mathbf{M}})$ in equation A.12. Since $det(\widehat{\mathbf{M}})$ is a third order polynomial in s, it is very difficult to find its roots analytically, unless some simplifying assumptions are made.

Let us assumes that $A_v(s)$ has a dominant pole p_o which is much lower than the other two non-dominant poles p_1 and p_2. The polynomial which gives the solutions for poles can be written as:

$$det(\widehat{\mathbf{M}}) = M_o\left(1 + \frac{s}{p_o}\right)\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) = M_o\left(1 + \frac{s}{p_o}\right)\left(1 + 2\xi_p\frac{s}{\omega_{op}} + \frac{s^2}{\omega_{op}^2}\right) \tag{A.22}$$

where M_o is a constant factor and

$$p_{1,2} = \xi_p \cdot \omega_{op} \pm \omega_{op}\sqrt{\xi_p^2 - 1} \tag{A.23}$$

Grouping the coefficients of s^0, s^1, s^2 and s^3, equation A.22 becomes:

$$\frac{det(\widehat{\mathbf{M}})}{M_o} = 1 + s\left(\frac{1}{p_o} + \frac{2\xi_p}{\omega_{op}}\right) + s^2\frac{2\xi_p}{\omega_{op}}\left(\frac{1}{p_o} + \frac{1}{2\xi_p \cdot \omega_{op}}\right) + s^3\frac{1}{p_o \cdot \omega_{op}^2} \tag{A.24}$$

Since p_0 is dominant, $p_o \ll 2\xi_p\omega_{op}$ and $p_o \ll \frac{\omega_{op}}{2\xi_p}$. Hence:

$$\frac{det(\widehat{\mathbf{M}})}{M_o} \cong 1 + s\frac{1}{p_o} + s^2\frac{2\xi_p}{\omega_{op}p_o} + s^3\frac{1}{p_o \cdot \omega_{op}^2} \tag{A.25}$$

From the analysis of the above equation, one can see that p_o, ω_{op} and ξ_p can be directly determined from the coefficients of the polynomial function $det(\widehat{\mathbf{M}})$. Supposing that $det(\widehat{\mathbf{M}}) = m_o + m_1 s + m_2 s^2 + m_3 s^3$, the expressions of p_o, ω_{op} and ξ_p are given by:

$$\begin{aligned} p_o &= \frac{m_o}{m_1} \\ \omega_{op}^2 &= \frac{m_1}{m_3} \\ \xi_p &= \frac{\omega_{op}}{2} \cdot \frac{m_2}{m_1} = \frac{1}{2} \cdot \frac{m_2}{\sqrt{m_1 m_3}} \end{aligned} \tag{A.26}$$

Calculation of the coefficients of *det*$(\widehat{\mathbf{M}})$

The coefficient m_o of the polynomial $det(\widehat{\mathbf{M}})$ is given by:

$$\begin{aligned} m_o &= -g_{ds2}g_{ds3}g_{load} - g_{m2}(g_{m3} + g_{ds3})g_{load} - (g_{load} + g_{ds2})g_{ds3}g_{ds1} \\ &= -g_{m2}g_{m3}\left\{g_{load}\left[1 + \frac{1}{a_{o3}} + \frac{1}{a_{o2}a_{o3}}\left(1 + \frac{g_{ds1}}{g_{ds2}}\right)\right] + \frac{g_{ds1}}{a_{o2}a_{o3}}\right\} \\ &\cong -g_{m2}g_{m3}g_{load} \end{aligned} \tag{A.27}$$

where a_{o2}, $a_{o3} \gg 1$ are the intrinsic gain expressions given by the equation A.17.

Following a similar approach, the coefficients m_1, m_2 and m_3 are given by:

$$\begin{aligned} m_1 &\cong -g_{m2}g_{m3}C_{load}^* = -g_{m2}g_{m3}\left(C_{load} + C_{gd2}\right) \\ m_2 &\cong -g_{m2}g_{m3}\left[\frac{C_{gs2}^*(C_{load} + C_{gd2})}{g_{m2}} + \frac{C_{gd2}(C_{load} + C_{gs3})}{g_{m3}}\right] \\ m_3 &\cong -\left(C_{load} + C_{gd2}\right)C_{gs2}^*C_{gs3}\left[1 + \frac{C_{load} \oplus C_{gd2}}{C_{gs2}^* \oplus C_{gs3}}\right] \end{aligned} \tag{A.28}$$

where $\oplus$ is the symbol for series connection of two capacitances, i.e $c_1 \oplus c_2 = \frac{c_1 c_2}{c_1 + c_2}$.

With m_o, m_1, m_2 and m_3 determined, the expressions of p_o, ω_{op} and ξ_p are:

$$\begin{aligned} p_o &= \frac{g_{load}}{C_{load}+C_{gd2}} \\ \omega_{op}^2 &= \frac{g_{m2}g_{m3}}{C^*_{gs2}C_{gs3}} \cdot \frac{1}{1+\frac{C_{load}\oplus C_{gd2}}{C^*_{gs2}\oplus C_{gs3}}} \\ \xi_p &= \frac{\omega_{op}}{2}\left[\frac{C^*_{gs2}}{g_{m2}} + \frac{C_{gd2}\left(C_{load}+C_{gs3}\right)}{g_{m3}\left(C_{load}+C_{gd2}\right)}\right] \end{aligned} \tag{A.29}$$

In order to check the assumption that p_o is dominant over p_1 and p_2, consider the following numerical example:

- $\mathbf{T_1}$: $g_{m1} = 700\mu S$, $g_{ds1} = 5\mu S$
- $\mathbf{T_2}$: $g_{m2} = 50\mu S$, $g_{ds2} = 1\mu S$, $C_{gs2} = 10fF$, $C_{gd2} = 5fF$
- $\mathbf{T_3}$: $g_{m3} = 10\mu S$, $g_{ds3} = 50nS$, $C_{gs3} = 30fF$, $C_{gd3} = 5fF$
- **Load**: $g_{load} = 20nS$, $C_{load} = 20fF$

The numerical values presented here are similar to the ones extracted with SPICE from the RGC amplifier circuit employed in the design of the DEPFET readout. The values of p_o, ω_{op} and ξ_p given by equation A.29 are:

$$\begin{aligned} p_o &= 800kHz \\ \omega_{op} &= 891MHz \\ \xi_p &= 0.58 \end{aligned} \tag{A.30}$$

Since $\xi_p < 1$, $p_{1,2}$ are two complex conjugate poles with the pole frequency ω_{op} much higher than the dominant pole p_o.

A.2.3 Analysis of the voltage transfer function

Having determined the position of the poles and zeros of the transfer function, equation A.13 can be written as:

$$A(s) = -\frac{g_{m1}}{g_{load}} \frac{\left(1-\frac{s}{z_1}\right)\left(1-\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_o}\right)\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} = -\frac{g_{m1}}{g_{load}} \frac{1+\frac{2\xi_z}{\omega_{oz}}s+\frac{s^2}{\omega_{oz}^2}}{\left(1+\frac{s}{p_o}\right)\left(1+\frac{2\xi_p}{\omega_{op}}s+\frac{s^2}{\omega_{op}^2}\right)} \tag{A.31}$$

where ω_{oz} and ξ_z, p_o, ω_{op} and ξ_p are given in the equations A.21 and A.29, respectively. One can see that the low frequency gain $A_o = A(0) = -\frac{g_{m1}}{g_{load}}$ is identical to what we obtained in section 5.3.1 from the low frequency analysis (see equation 5.42).

The poles of the amplifier are all situated in the left half of the complex plane irrespective to the values of all the transistor parameters. The condition that the zeros are situated in the left half of the plane is (to avoid negative phase shift):

$$\xi_z > 0 \Rightarrow g_{m2} > g_{m3} \tag{A.32}$$

With the numerical values considered in the previous sub-section, the frequency dependence of the magnitude and phase of the amplifier transfer function from equation A.31 are plotted in Figure A.6 (the red curves). The blue curves show the same quanti-

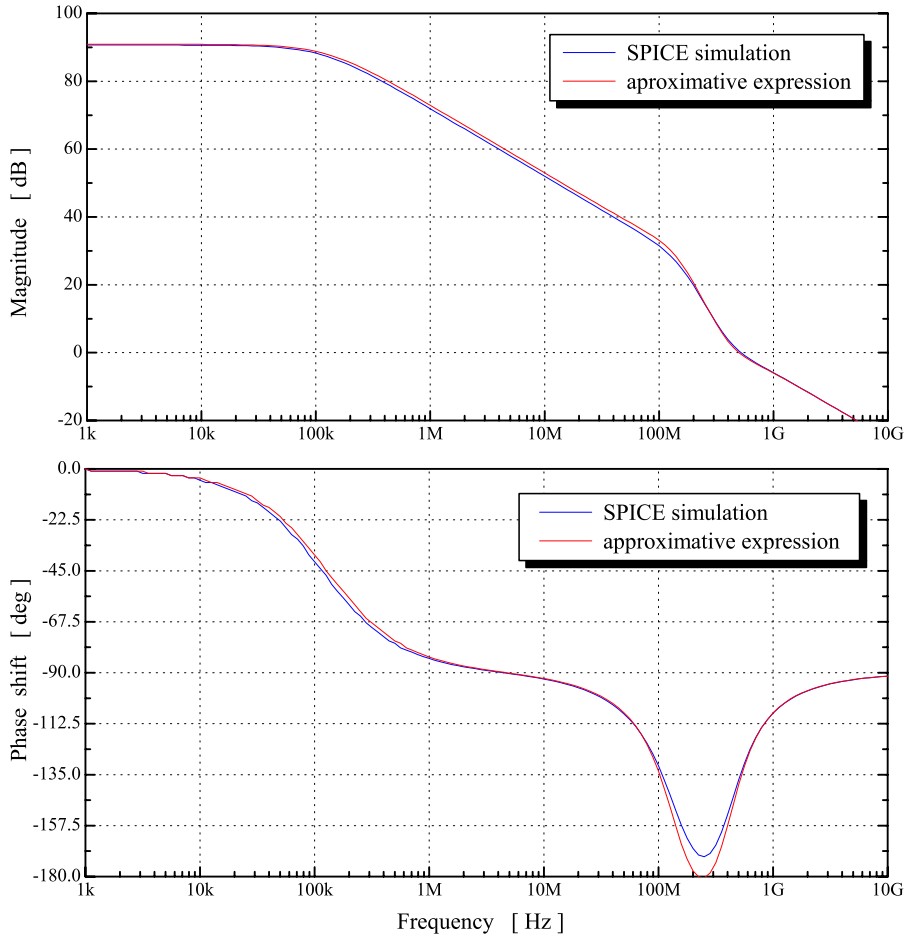


Figure A.6: Magnitude and phase of the RGC transfer function.

ties obtained from the SPICE simulation of the circuit in Figure A.5. One can see that the curves are in good agreement, confirming that the approximative method of finding the poles and zeros gives reliable results.

Regarding the effect of the capacitance C_{gd1} which has been neglected during the analysis, Figure A.7 shows the the results of the SPICE simulations of the circuit in Figure A.5a with and without including C_{dg1}. One can see that a positive zero occurs at very high frequency, well beyond the 0 dB frequency. This will not affect the stability of the amplifier.

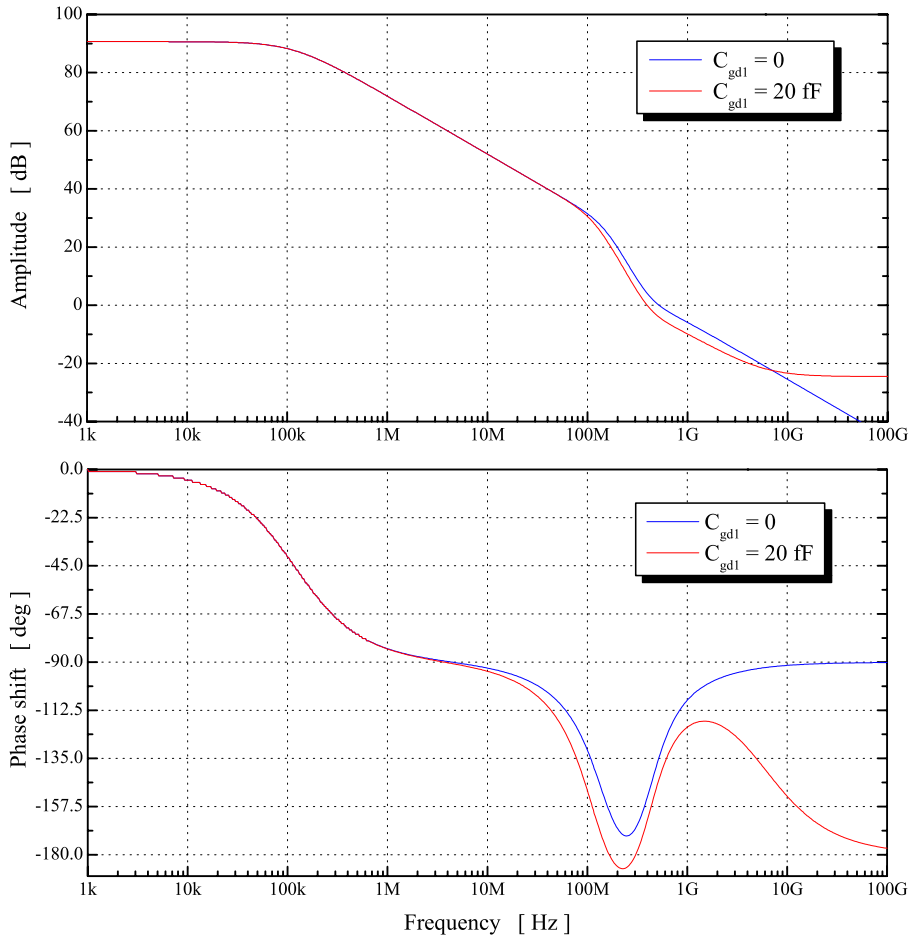


Figure A.7: Effect of C_{gd1} on the magnitude and phase of the RGC transfer function.

A.2.4 Stability of the the RGC amplifier: frequency compensation

It can be observed in Figure A.6 and A.7 that the phase shift nears the values of -180^o at a frequency where the magnitude is larger than 1; oscillations at this frequency can occur. The amplifier must be compensated, i.e. enough phase margin must be ensured in order to avoid unwanted oscillations.

The simplest way of doing this would be to increase the value of the load capacitance C_{load} until the distance between the dominant pole p_o (inverse proportional to C_{load}) and the complex conjugate poles $p_{1,2}$ (slow varying with C_{load}) is large enough to ensure the desired phase margin. The amplifier bandwidth is drastically reduced in this case.

A better compensation scheme is found by analyzing the expressions of the zeros and poles determined in the previous sub-sections. One can see that the zero frequency ω_{oz} can be moved toward the non-dominant poles frequency ω_{op} (smaller than ω_{oz}) by increasing the value of C_{gd2}. The negative phase shift introduced by the non-dominant poles is balanced by the positive phase shift of the zeros. Figure A.8 shows the magnitude and

the phase of the transfer function for different values of C_{gd2}. One can see that the phase

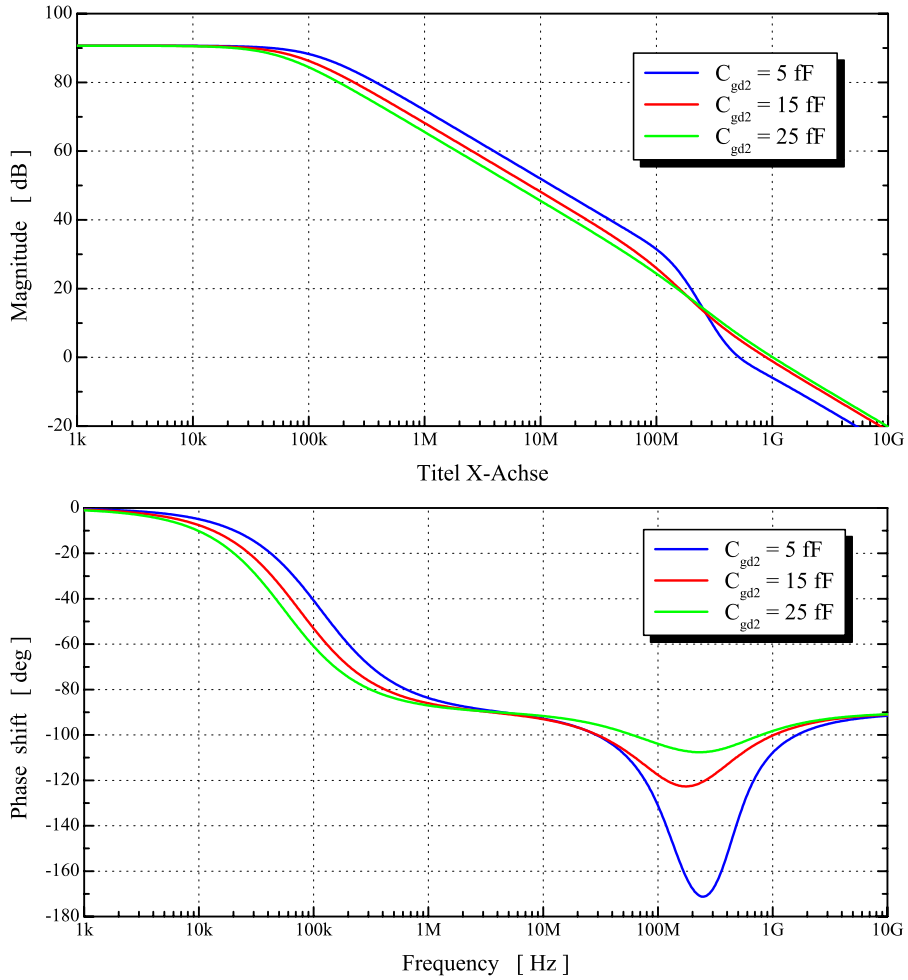


Figure A.8: Magnitude and phase of the RGC transfer function for various values of C_{gd2}.

margin (distance to the -180^o limit) is increased at the small price of reducing slightly the amplifier bandwidth (p_o decreases also with C_{gd2}). This is the compensation method used in the design of the RGC amplifier for the DEPFET readout circuit (see also the simulation results in Figure 5.16).

Appendix B

Calculation of A_1, A_2, A_3 for an n^{th} order filter

Consider the characteristic transfer function of a semi-gaussian filter of n^{th} order:

$$H(s) = \frac{s\tau}{(1+s\tau)^{n+1}} \tag{B.1}$$

where $s = j\omega$ is the complex frequency and τ is the time constant of the filter. The coefficients A_1, A_2 and A_3 employed in the theoretical noise calculations performed in section 4.3 are given by:

$$\begin{aligned} A_1 &= \frac{1}{2\pi} \frac{\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x^2} dx}{max^2\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right)} \\ A_2 &= \frac{1}{2\pi} \frac{\int_0^\infty |H(\frac{jx}{\tau})|^2 dx}{max^2\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right)} \\ A_3 &= \frac{\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x} dx}{max^2\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right)} \end{aligned} \tag{B.2}$$

The inverse Laplace transform of $\frac{H(s)}{s}$ is found as:

$$\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\} = \frac{1}{\tau^n}\mathcal{L}^{-1}\left\{\frac{1}{\left(s+\frac{1}{\tau}\right)^{n+1}}\right\} = \frac{1}{n!}\left(\frac{t}{\tau}\right)^n e^{-\frac{t}{\tau}} \tag{B.3}$$

This function has a maximum at $t = n\tau$, whose value is:

$$max\left(\mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}\right) = \frac{n^n}{e^n n!} \tag{B.4}$$

Coefficient A_1

The numerator in the expression of A_1 is:

$$\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x^2} dx = \int_0^\infty \frac{dx}{(1+x^2)^{n+1}} \tag{B.5}$$

With the change of variable $x = \sqrt{u}$, the integral in the above equation is given by:

$$\int_0^\infty \frac{dx}{(1+x^2)^{n+1}} = \frac{1}{2}\int_0^\infty \frac{u^{-1/2}du}{(1+u)^{n+1}} = \frac{1}{2}B\left(\frac{1}{2}, n+\frac{1}{2}\right) \tag{B.6}$$

where $B(p,q)$ is Beta function and is given by:

$$\begin{aligned} B(p,q) &= \int_0^1 x^{p-1}(1-x)^{q-1}dx = \int_0^\infty \frac{u^{p-1}}{(1+u)^{p+q}}du \quad \text{with } x = \frac{u}{u+1} \\ &\text{and} \\ B(p,q) &= \frac{\Gamma(p)\Gamma(q)}{\Gamma(p+q)}, \quad p,q>0 \end{aligned} \tag{B.7}$$

where $\Gamma(x)$ is Gamma function. Using the above relation between Beta and Gamma functions:

$$B\left(\frac{1}{2}, n+\frac{1}{2}\right) = \frac{\Gamma\left(\frac{1}{2}\right)\Gamma\left(n+\frac{1}{2}\right)}{\Gamma(n+1)} = \frac{\pi(2n-1)!!}{2^n n!} \tag{B.8}$$

where $(2n-1)!! = 1\cdot 3\cdot 5\cdot ...\cdot (2n-1)$. The coefficient A_1 is therefore obtained as:

$$\boxed{A_1 = \frac{1}{4\pi}\cdot\frac{e^{2n}(n!)^2}{n^{2n}}\frac{\pi(2n-1)!!}{2^n n!} = \frac{e^{2n}n!\cdot(2n-1)!!}{2^{n+2}n^{2n}}} \tag{B.9}$$

Coefficient A_2

The numerator in the expression of A_2 is:

$$\int_0^\infty \left|H\left(\frac{jx}{\tau}\right)\right|^2 dx = \int_0^\infty \frac{x^2}{(1+x^2)^{n+1}}dx \tag{B.10}$$

With the change of variable $x = \sqrt{u}$, the integral in the above equation is given by:

$$\int_0^\infty \frac{x^2}{(1+x^2)^{n+1}}dx = \frac{1}{2}\int_0^\infty \frac{u^{1/2}du}{(1+u)^{n+1}} = \frac{1}{2}B\left(\frac{3}{2}, n-\frac{1}{2}\right) \tag{B.11}$$

Since:

$$B\left(\frac{3}{2}, n-\frac{1}{2}\right) = \frac{\Gamma\left(\frac{3}{2}\right)\Gamma\left(n-\frac{1}{2}\right)}{\Gamma(n+1)} = \frac{\pi(2n-3)!!}{2^n n!} \tag{B.12}$$

the coefficient A_2 is given by:

$$\boxed{A_2 = \frac{e^{2n}n!\cdot(2n-3)!!}{2^{n+2}n^{2n}} = \frac{A_1}{2n-1}} \tag{B.13}$$

Coefficient A_3

The numerator in the expression of A_3 is:

$$\int_0^\infty \frac{|H(\frac{jx}{\tau})|^2}{x} dx = \int_0^\infty \frac{x}{(1+x^2)^{n+1}} dx \tag{B.14}$$

With $x = \sqrt{u}$, the integral in the above equation becomes:

$$\int_0^\infty \frac{x^2}{(1+x^2)^{n+1}} dx = \frac{1}{2} \int_0^\infty \frac{du}{(1+u)^{n+1}} = \frac{1}{2} B(1,n) \tag{B.15}$$

But

$$B(1,n) = \frac{\Gamma(1)\Gamma(n)}{\Gamma(n+1)} = \frac{1}{n} \tag{B.16}$$

Therefore, the coefficient A_3 is given by:

$$\boxed{A_3 = \frac{e^{2n}(n!)^2}{2n^{2n+1}}} \tag{B.17}$$

Appendix C

Data sheets

The design parameters of the readout building blocks are presented in this chapter.

C.1 DEPFET bias current source

The design parameters of the DEPFET bias current source (refer to Figure 5.2 in Chapter 5) are listed in the Table C.1.

Component / Type	**Description**	**Value**
T_1 / PMOS	Diode connected transistor	W/L $[\mu m] = 15/3$
T_2 / PMOS	Output transistor	W/L $[\mu m] = 9/3$
R / RPOLY	Reference resistor	1028 Ω

Table C.1: Design parameters of the DEPFET bias current source

C.2 Feedback amplifier

The design parameters of the feedback amplifier (refer to Figure 5.18) are listed in Table C.2.

Transistor / Type	**Description**	**W/L** [μm]
T_1 / NMOS	Input transistor	76.8/0.6
T_2 / PMOS	Cascoding transistor	12.4/0.6
T_3 / PMOS	Regulating transistor	8/2
T_4 / PMOS	Source-follower	6/0.6
T_{fb} / NMOS	Feedback transistor	1/20
T_{b1} / PMOS	Bias of T_1	8/3
T_{1b2} / NMOS	Load current source	4/1
T_{2b2} / NMOS	Load current source	6.2/2
T_{b3} / NMOS	Bias of T_3	5/4
T_{b4} / PMOS	Bias of T_4	6.2/2
Capacitance / Type	**Description**	**Value**
C_{in} / CPOLY	Input capacitance	500 fF
C_{fb} / CPOLY	Feedback capacitance	25 fF
C_c / CPOLY	Compensation capacitance	30 fF
Current source	**Description**	**Typical value**
$I_{b,in}$	Bias current of T_1	40 μA
I_{load}	Bias current of T_2	2.7 μA
I_{rgc}	Bias current of T_3	1 μA
I_{sf}	Bias current of T_4	2.7 μA

Table C.2: Design parameters of the feedback amplifier

C.3 CR-RC shaper

The design parameters of the CR-RC shaper from Figure 5.25 are given in Table C.3

Transistor / Type	**Description**	**W/L** [μm]
T_1 / NMOS	Input transistor	0.8/79.4
T_2 / NMOS	Mirror of T_1	0.8/10
T_3 / PMOS	Load of T_2	2/2
T_4 / PMOS	Mirror of T_3	2/8.4
T_5 / NMOS	Output transistor	0.8/79.4
Capacitance	**Description**	**Value**
C_1	Input capacitance	500 fF
C_2	Output capacitance	750 fF
Current source	**Description**	**Typical value**
$I_{b,sh}$	Bias current of T_1	100 nA

Table C.3: Design parameters of the CRRC shaper

C.4 Shaper based on OTAs

The design parameters of the operational transconductance amplifier (OTA) from Figure 5.32 employed in the design of the shaper circuit of Figure 5.31 are listed in Table C.4.

Transistor / Type	**Description**	**W/L** [μm]
T_1, T_2 / NMOS	Differential pair	1/6
T_3, T_4 / PMOS	Load of the differential pair	8/2
T_5 / PMOS	Mirror of T_3	2/2
T_6 / PMOS	Mirror of T_4	1/16
T_7 / NMOS	Load of T_5	2/4
T_8 / NMOS	Mirror of T_7	1/23.5
Current source	**Description**	**Typical value**
$I_{b,ota}$	Bias current of OTA	10 μA

Table C.4: Design parameters of the symmetrical OTA.

C.5 Output buffers

The parameters of the transistors employed in the design of the analog output buffer (see Figure 5.35) are listed in Table C.5 (amplifier output buffer) and Table C.6 (shaper output buffer).

Transistor / Type	**Description**	**W/L** [μm]
T_1 / NMOS	Source follower	19.8/0.6
T_{b1} / NMOS	Bias of T_1	20/1.3
T_{b2} / NMOS	Mirror of T_{b1}	12.3/2
T_{b3} / PMOS		2.6/4

Table C.5: Design parameters of the amplifier output buffer.

Transistor / Type	**Description**	**W/L** [μm]
T_1 / NMOS	Source follower	20/0.6
T_{b1} / NMOS	Bias of T_1	6.2/2
T_{b2} / NMOS	Mirror of T_{b1}	12.3/2
T_{b3} / PMOS		1.4/4

Table C.6: Design parameters of the shaper output buffer.

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Acknowledgements

This work has been carried out at the Department of Physics at University of Siegen in co-operation with the Semiconductor Laboratory of the Max-Plank-Institute for Extraterrestrial Physics in Garching.

First of all, I owe my sincere and deepest gratitude to my supervisor, Prof. Martin Holder for his support, valuable ideas, his advice and trust in me during this research. I also thank him for helping me in receiving the financial support which was important for my study.

I would also like to thank Prof. Gerhard Lutz, Prof. Lothar Strüder and Dr. Rainer Richter from the Semiconductor Laboratory of MPI Garching, who provided the detector structures studied in this work. I am very grateful for their help and valuable advices on DEPFET detector operation. A special thank to Dr. Peter Klein who introduced me into this detector concept.

I wish to thank the actual and former members of Prof. Holder's research group for their willingness of helping me and for the enjoyable work atmosphere. Especially, I want to express my gratitude to Dr. Michal Ziolkowski and Dr. Joachim Hausmann for their help and guidance during the work with CADENCE Design Framework Program. The members of Prof. Walenta's research group deserve also special thanks for the constructive discussions that we have had.

Last but not the least, I would like to thank my family - my wife Dana and my twins Andrei and Cristiana for their patience, understanding and support throughout the period of the work.